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Cite as: Rev. Sci. Instrum. **92**, 103502 (2021); <https://doi.org/10.1063/5.0057318>

Submitted: 19 May 2021 • Accepted: 15 September 2021 • Published Online: 06 October 2021

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ABSTRACT

For the first time, a digital Mirror Langmuir Probe (MLP) has successfully sampled plasma temperature, ion saturation current, and floating potential together on a single probe tip in real time in a radio-frequency driven helicon linear plasma device. This is accomplished by feedback control of the bias sweep to ensure a good fit to I–V characteristics with a high frequency, high power digital amplifier, and field-programmable gate array controller. Measurements taken by the MLP were validated by a low speed I–V characteristic manually collected during static plasma conditions. Plasma fluctuations, induced by varying the axial magnetic field ($\tilde{f} = 10$ Hz), were also successfully monitored with the MLP. Further refinement of the digital MLP pushes it toward a turn-key system that minimizes the time to deployment and lessens the learning curve, positioning the digital MLP as a capable diagnostic for the study of low radio-frequency plasma physics. These demonstrations bolster confidence in fielding such digital MLP diagnostics in magnetic confinement experiments with high spatial and adequate temporal resolution, such as edge plasma, scrape-off layer, and divertor probes.

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I. INTRODUCTION

The Langmuir probe is a workhorse diagnostic for studying the edge of fusion plasma devices, such as tokamaks and stellarators. The digital Mirror Langmuir Probe (MLP) is continuing to be developed by a joint collaboration between the University of Liverpool UK, the United Kingdom Atomic Energy Authority (UKAEA), and the MIT Plasma Science and Fusion Center for deployment on MAST-U with the goal of researching turbulent transport. However, much of the important physics happens at time scales faster than those that the traditional Langmuir probe biasing techniques can capture. This limitation is due to the need to sweep the voltage at which the probe is biased in order to construct the full I–V characteristic used to determine the electron temperature (T_e), density (n_e), and floating potential (V_f).¹ Triple probes have been used to collect Langmuir probe measurements with high time resolution but at the cost of spatial resolution. However, if one knows the expected T_e , then it is possible to optimize three bias voltage states on a single probe tip and still extract accurate measurements of the plasma parameters. For such a bias scheme to be possible, it is necessary to determine the plasma temperature in real time and adapt the bias states accordingly. This is the approach of the Mirror Langmuir Probe

(MLP) biasing system, and has been successfully implemented with analog electronics on Alcator C-Mod with a high time resolution (1.1 MHz).²

More recently, work has been carried out to implement the real-time calculation and bias control in digital Field-Programmable Gate Array (FPGA)-based electronics. The first implementation of such a digital MLP controller, as reported by Vincent *et al.*,³ was not tested using a real probe in the plasma, but only against a second digital FPGA system that simulated the response of a probe in the plasma.

This paper reports on the first successful adaptation of the FPGA MLP controller for diagnosing a real laboratory plasma. Specifically, the probe was tested in both stable and fluctuating plasma conditions with approximate time-averaged values of $\langle T_e \rangle \sim 8$ eV, $\langle n_e \rangle \sim 2.3 \cdot 10^{17} \text{ m}^{-3}$, and $\langle V_f \rangle \sim -4.5$ V. The probe measurements in stable plasma conditions were compared to the time-averaged measurements, which were determined using a full I–V characteristic collected manually with a variable voltage supply and a multimeter.

This paper is organized as follows: Sec. II discusses the MLP algorithm implemented in the FPGA logic. Section III discusses the system used to drive the probe in the plasma and the DIONISOS

linear plasma device. Section IV reports on the results of the first set of real plasma tests of the probe.

II. THE MLP ALGORITHM

The MLP algorithm starts by picking three bias states that are optimized to the plasma conditions assumed for some initial guess based on either expected electron temperature or a prior measurement of temperature. This optimization ensures a good fit to the following Langmuir probe equation:⁴

$$I_{LP} = I_{sat} \left(e^{\frac{(V_{pr} - V_f)}{T_e}} - 1 \right), \quad (1)$$

where I_{sat} is the ion saturation current at large negative biases, V_{pr} is the applied bias to the probe, V_f is the floating potential, and T_e is the electron temperature for the lower part of the bias sweep before the rollover of the I–V characteristic occurs. Ideally, the three applied bias states draw currents through the probe for $-I_{sat}$, zero current, and $+I_{sat}$, similar to the triple probe operation. Applying the optimal bias states is simplified by capacitive coupling, as shown in Fig. 1, between the probe and the voltage driver. When the V_{pr} is not optimal such that the time-averaged current is not zero, the capacitor charges up to near (or ideally at) V_f by the differential current draw. The probe bias can then be expressed as the sum of the capacitor voltage, V_c , and the externally applied biases as follows:

$$V_{pr} = V_{\mp,0} + V_C, \quad (2)$$

where $V_{\mp,0}$ corresponds to the three bias states. Solving the Langmuir probe equation simultaneously around $I_{LP} = 0.964I_{sat}$ and $-0.964I_{sat}$ finds that the necessary applied biases for these optimal states are³

$$V_- = -3.325T_e, \quad (3a)$$

$$V_+ = 0.675T_e, \quad (3b)$$

$$V_0 = 0. \quad (3c)$$

The chosen values of current are less than I_{sat} in order to reduce the magnitude of V_- necessary to achieve it. A new value of one of the

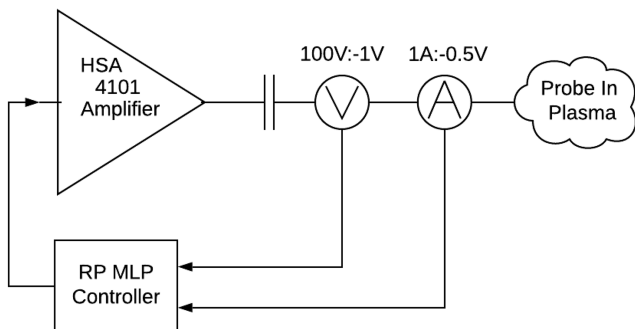


FIG. 1. Schematic of the Langmuir probe system used to drive the voltage and measure probe bias and current. A 100 V bias across the voltmeter produces a signal of -1 V. In addition, a 1 A current through the ammeter produces a signal of -0.5 V at the MLP.

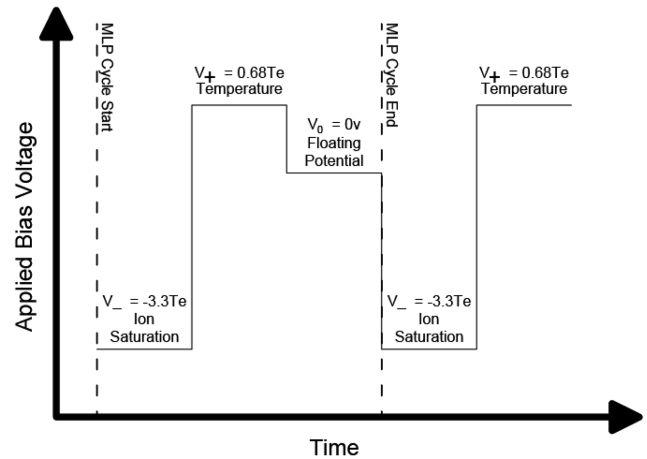


FIG. 2. The bias states of the MLP algorithm. At each of the three bias states, a different plasma parameter is updated to a new value.

plasma parameters is calculated at each of the three bias states using the following rearranged Langmuir probe equation:

$$I_{sat} = \frac{I_{LP}}{\left(\exp\left(\frac{V_{pr} - V_F}{T_e}\right) - 1 \right)} : V_{pr} = V_- + V_C, \quad (4a)$$

$$T_e = \frac{(V_{pr} - V_F)}{\ln\left(\frac{I_{LP}}{I_{sat}} + 1\right)} : V_{pr} = V_+ + V_C, \quad (4b)$$

$$V_F = V_{pr} - T_e \ln\left(\frac{I_{LP}}{I_{sat}} + 1\right) : V_{pr} = V_C, \quad (4c)$$

where V_{pr} is the total voltage on the probe and is a directly measured experimental quantity (this may slightly differ from the imposed V_{pr} due to cable capacitance, pickup voltages, etc.,) and I_{LP} is the measured current drawn by the probe. The ordering of the bias states and calculations is shown in Fig. 2. Note that while the optimization was based on the assumption of the capacitor voltage equal to the floating potential, the algorithm does not require this to be true in order to calculate the temperature accurately, as the calculation uses the real voltage–current pair at the probe tip. As such, the capacitor is only necessary for the ease of driving the bias, not for the real-time calculation.

A full description of the algorithm implemented in FPGA-based electronics can be found in Ref. 3, while a treatment of the analog approach is found in Ref. 5.

III. EXPERIMENTAL SETUP

A. Langmuir probe drive and control system

The MLP controllers were implemented on StemLabs Red Pitaya; however, other off-the-shelf FPGA boards could be used. The Red Pitaya integrates a Xilinx Zynq 7010 FPGA with two 125 MHz 14-bit analog-to-digital converters (ADCs), two 125 MHz 14-bit digital-to-analog converter (DACs), and a Dual-Core ARM Cortex-A9 MPCore microprocessor. The Koheron software

development kit's framework and memory management cores were extensively used in the configuration and build of the FPGA logic.³ The ADCs were used to monitor the probe current and voltage, and one DAC was used to send the requested voltage to a NF Corp HSA 4101 RF amplifier, which has a peak-to-peak voltage range of 142 V and slew rate of 5000 V/ μ s. The Langmuir probe was capacitively coupled to the amplifier using a variable capacitor, and measurements of the current and voltage on the probe took place on the "plasma side" of the coupling capacitor. A schematic of the circuit is shown in Fig. 1. The Langmuir probe electrode was a 25 mm diameter tungsten plate placed at one end of the 40 mm diameter plasma column, as shown in Fig. 3. Real-time calculation and bias selection are carried out on the FPGA chip. The hardware description language used to configure the FPGA for these calculations is available at <https://github.com/Rondin119/MIT-mirror-langmuir-probe-Dionisos>.

The FPGA hardware and configuration employed in this implementation limit the best achievable time resolution of measurements to \sim 800 kHz, mostly due to the time needed to calculate the division in the MLP equations. However, the frequency was intentionally limited to \sim 140 kHz during these tests to account for uncertainties in the stability of the calculation and the time response of the drive system. The MLP cycle time is readily reconfigured by changing the number of clock cycles allocated to each bias state in the high-level software configuration of the device, with an approximate theoretical minimum of \sim 55 clock cycles needed per level to complete the calculations. The FPGA logic has not been optimized with respect to clock cycles, so this lower limit could be pushed down in such an optimization.

At the conclusion of each bias level, the voltage-current pair at the probe tip is saved into the memory on the FPGA board and transferred via a First In First Out (FIFO) FPGA buffer to the Red Pitaya RAM (see the Appendix). As such, the Red Pitaya serves as both the controller and digitizer in this experiment. An I-V characteristic is then fit to these saved voltage-current pairs in post-processing to extract the plasma parameters. The real-time values of the plasma parameters calculated in the FPGA, used for the adaptive control, are likewise saved at the conclusion of the three bias state sweep. This allows for a direct comparison between the real-time

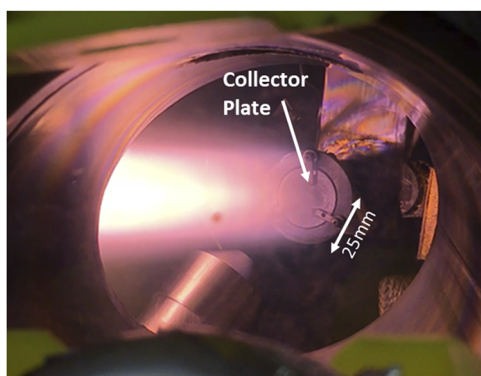


FIG. 3. The collector disk at the end of the plasma column that was used as the Langmuir probe electrode.

values and values extracted via a more traditional Langmuir probe analysis.

B. DIONISOS

DIONISOS is a linear plasma device coupled to a 1.7 MV tandem ion accelerator used to study plasma-material interactions (PMIs)⁶ (Fig. 3). The helicon plasma source is driven by a 13.56 MHz RF power supply coupled to the plasma with a Nagoya type III antenna and immersed in a magnetic field of up to 0.1 T with a set of Helmholtz coils. The plasma column is confined to an \sim 40 mm diameter from the plasma source tube. Normal plasma temperatures and ion fluxes are 2–6 eV and 10^{21} m⁻² s⁻¹, respectively. For PMI tests, materials under study are electrically isolated for variable biasing and sit at the intersection of the ion beam and plasma column. For the MLP tests, the ion beam was not used.

IV. REAL PLASMA EXPERIMENTS

Two tests of the MLP were performed. First, the plasma control parameters of RF power, magnet current, and gas flow were held constant, while the MLP controller swept the bias on the probe. For comparison, measurements were taken using a manually adjustable voltage supply and a multimeter in place of the MLP with the same probe electrode, converting the electrode into a standard swept Langmuir probe. The second test of the MLP was performed by programming a time-varying magnetic coil current, which caused time-varying plasma parameters at the same frequency. The fluctuation was limited to 10 Hz due to the magnet power supply and coil inductance, but the implemented MLP time resolution was much higher, i.e., \sim 140 kHz (7 μ s) for a full three bias cycle (Fig. 2).

A. Stable plasma tests

For the first test of the MLP, the results are shown in Fig. 4. The real-time algorithm required \sim 90 μ s to lock onto a stable value. The real-time floating potential converged first, preceding the electron temperature and ion saturation current by \sim 40 μ s. Real-time and post-processing values overlay perfectly after the real-time algorithm converged. The converged floating potential value was -3 V, the I_{sat} was 0.25 A, and the electron temperature was 10 eV.

The manually collected I-V characteristic fit with Eq. (1) is shown in Fig. 5. The characteristic shows clear evidence of the I-V rollover before negative ion saturation current is achieved.⁷ Restricting the fit to the lower portion of the I-V characteristic gives an estimate of floating potential as -4.6 V, I_{sat} as 0.25 A, and temperature as 7.4 eV. The early I-V rollover means that the current is no longer accurately predicted by the Langmuir probe equation used in the derivation of the algorithm and used for fitting during post-processing of the MLP data for the entire range of optimized biases. As a result, the MLP will overestimate plasma temperature in this experiment, explaining the discrepancy between the MLP temperature and manual temperature. Even so, since the I-V rollover is weak in this case, the MLP can still accurately track changes in temperature despite the absolute magnitude being overestimated.

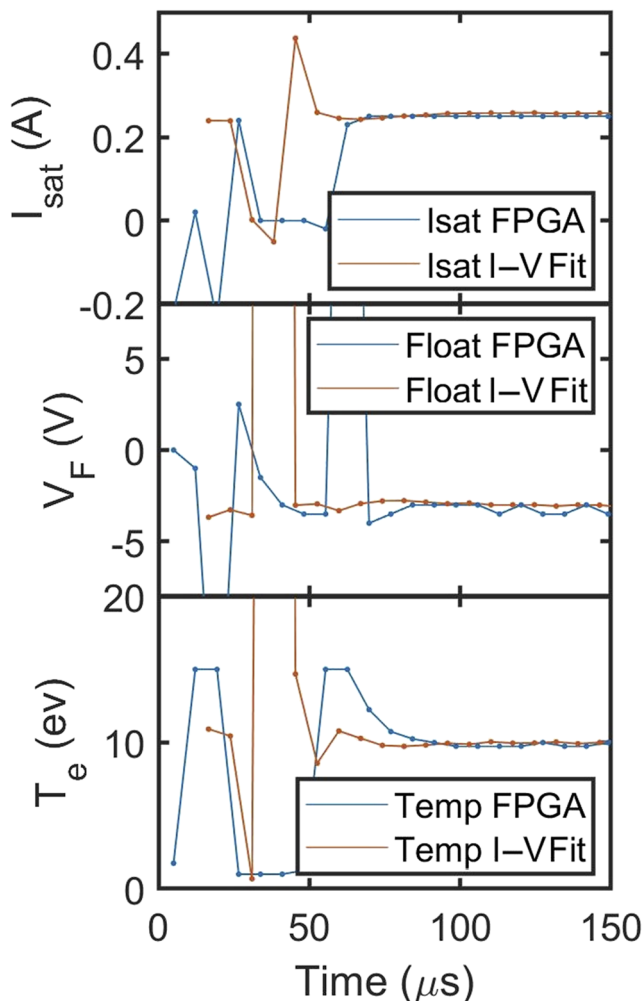


FIG. 4. Plasma conditions were held constant while MLP was triggered. “ I_{sat} /Float/Temp FPGAs” are the results of the calculation carried out on the FPGA, while “ I_{sat} /Float/Temp I–V Fit” is the post-processing fit of the I–V characteristic of the saved current and bias state. All three signals lock onto stable values within 90 μs . The algorithm takes several cycles to lock on. The ion saturation current locks onto ~ 0.25 A, floating potential locks onto ~ -3 V, and temperature locks onto ~ 10 eV. The post-processing fit produces nearly identical results to the real-time calculation.

A simple criterion to measure the impact of the I–V rollover is the magnitude of the current drawn by the probe when the system is in the floating state. If the real-time FPGA plasma parameters are constant, a consistently drawn current at the V0 state would indicate that the algorithm is not selecting optimal biases and that Eq. (1) has broken down, with a larger current indicating worse breakdown. This problem could be alleviated in future tests by solving Eq. (1) around lower probe currents, reducing the required bias range to try and avoid the rollover. In fact, the FPGA could be designed to switch between several different sets of “optimal” bias states if it detects a persistent non-zero “floating” current. However, it is not known what effect this would have on the stability of the real-time calculation. In addition, if the bias range is reduced too far, the

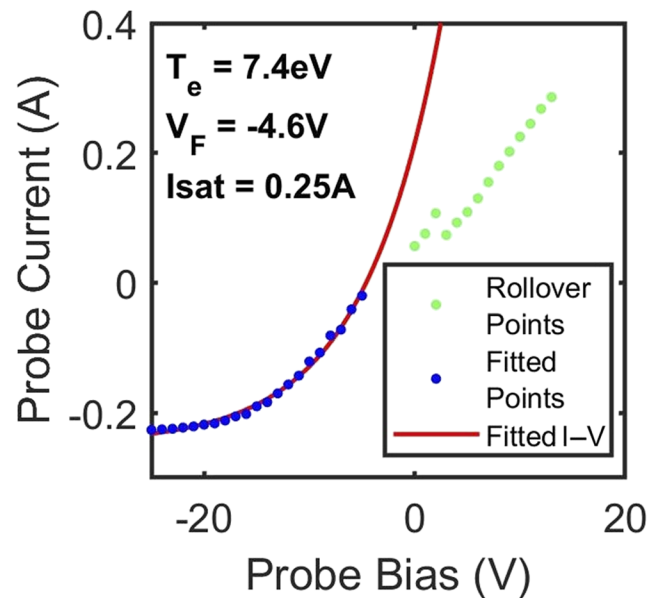


FIG. 5. Manually constructed I–V characteristic taken using a multimeter and variable voltage source. The I–V characteristic shows signs of rolling over into the electron saturation regime before the inverse of the ion saturation current is reached. In order to make a comparison to real-time MLP results, a fit is applied only to points at a lower probe bias, marked in blue, while points at higher probe bias, marked in green, are excluded. The fit so-obtained, as well as the results of the real-time MLP algorithm, will overpredict the plasma temperature due to the mismatch of the real I–V characteristic with Eq. (1).

three bias–current pairs become very close in the bias–current space, which will degrade the quality of the fit and increase the fit sensitivity to noise in the measurements.

B. Fluctuating plasma tests

In the second test, two frequencies were used to program the current output of the magnetic coil current: 10 Hz (Fig. 6) and 20 Hz (Fig. 7). In both cases, the MLP clearly tracks the oscillation in plasma parameters at the drive frequency. The programmed current amplitude used in both cases was the same. However, the amplitude of the fluctuation in the plasma parameters decreased when the frequency increased. This may indicate that the magnet power supply is insufficient to fully overcome the magnetic coil inductance, setting an upper limit on the fluctuation frequency.

The MLP real-time calculations are systematically lower and have less precision than the fit values due to the manner in which the real-time calculations are saved. The details of how the real-time data are saved by the Red Pitaya (see the Appendix) necessitated that a divide-by-32 be applied in the real-time FPGA bit value of floating potential and ion saturation current and a divide-by-16 be applied to the real-time bit values for temperature prior to saving in RAM. These values are rounded down, causing the perceived downshift in values. Within the FPGA implementation of the algorithm, full precision is used, and thus, it is expected that those values match the post-processed ones much more closely. It is unclear that what part of the large scatter present in both the fitted values and real-time

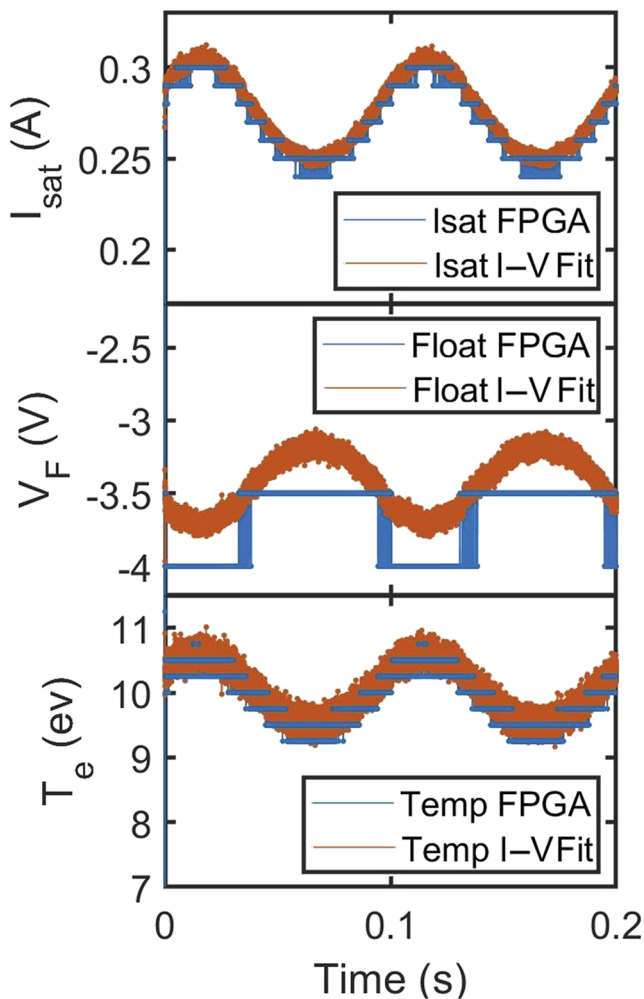


FIG. 6. MLP was triggered simultaneously with a 10 Hz fluctuation in the DIONISOS magnetic field strength. “ I_{sat} /Float/Temp FPGAs” are the results of the calculation carried out on the FPGA, while “ I_{sat} /Float/Temp I–V Fit” is the post-processing fit of the I–V characteristic of the saved current and bias state. Clear variations are seen in all three plasma parameters tracked well by both real-time calculations and post-processing fits. The large quantization steps for the real-time calculation are caused by a divide-by-32 on V_f and I_{sat} and a divide-by-16 on T_e during saving. All real-time values are rounded down during saving, resulting in the real-time values being systematically lower than the post-process results.

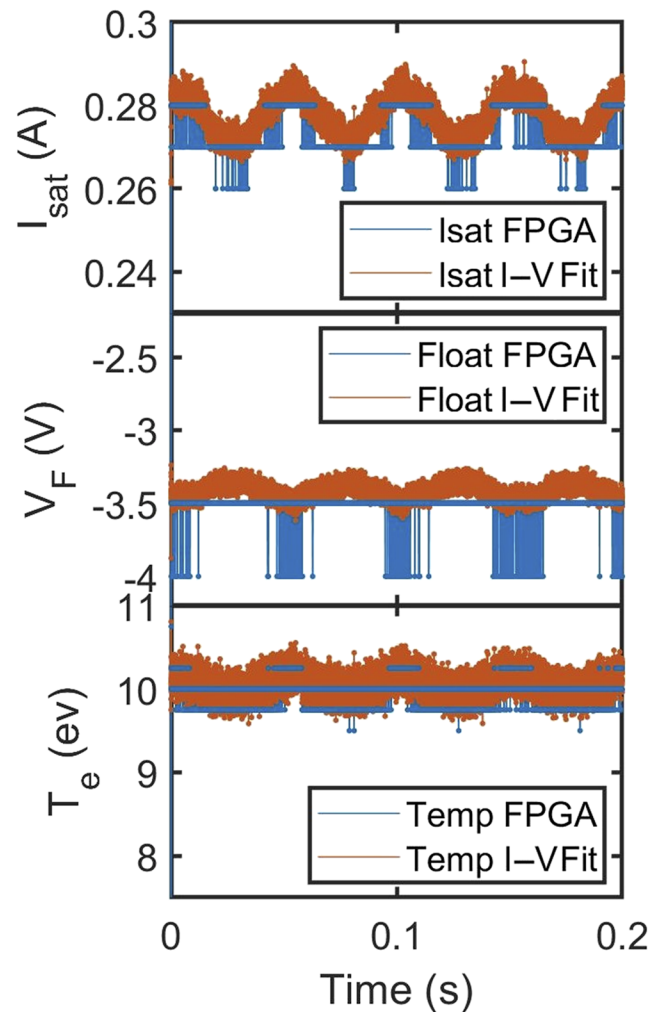


FIG. 7. MLP was triggered simultaneously with a 20 Hz fluctuation in the magnetic field strength. “MLP I_{sat} /Float/Temp FPGAs” are the results of the calculation carried out on the FPGA, while “MLP I_{sat} /Float/Temp I–V Fit” is the post-processing fit of the I–V characteristic of the saved current and bias state. The programmed fluctuation amplitude was held constant from the 10 Hz test, but plasma fluctuation was a much smaller amplitude. This is evidence that the magnet power supply and inductance are insufficient to perform the full magnetic field fluctuation programmed. Post-process and real-time calculations agree well.

values is due to real plasma fluctuations vs due to the error in the quantization and fitting.

As noted previously, DIONISOS is driven by a 13.56 MHz RF source, and thus, we expect interesting dynamics on this time scale. While this is well above the theoretical maximum time resolution for the digitization of data, it is a factor of 10 slower than the ADC conversion rate of the Red Pitaya and maximum clock speed of the FPGA. Therefore, it is possible, in principle, to phase lock the measurements of the plasma parameters to the RF signal and learn about the dynamics of the plasma at that frequency. Additional work is planned along these lines.

V. CONCLUSION

A digital mirror Langmuir probe drive controller was implemented on a commercial FPGA board and tested on the DIONISOS linear device for real plasma parameter measurements. Two tests were conducted to determine functionality: first, the MLP results were compared with a manually collected I–V characteristic using the same probe tip in steady plasma conditions; second, an artificial fluctuation was induced at a known frequency in the plasma and the MLP was used to track it.

When the plasma conditions were held fixed, the MLP estimates for the plasma parameters showed good agreement with the estimates obtained via the manually collected I–V characteristic

except for a discrepancy that can be explained by an early rollover in the I–V characteristic. The real-time MLP calculations and the post-processing fits carried out on the MLP data showed near perfect agreement.

When a low-frequency fluctuation was induced in the plasma, the MLP was able to track it with high fidelity. The fluctuation frequency was limited by the inductance of the magnet and the magnet power supply.

The digital FPGA mirror Langmuir probe controller was able to replicate the functionality of the original analog mirror Langmuir probe, albeit at a reduced frequency, in a real plasma environment. It is capable of calculating the plasma temperature, floating potential, and ion saturation current in real time and adjusting the bias states of the three-point probe sweep. The use of primarily off-the-shelf components allowed for rapid setup and deployment. This demonstrates that the digital mirror Langmuir probe can be a powerful diagnostic for studying plasma turbulence in the low RF range. The digital MLP is continuing to be developed by a joint collaboration between the University of Liverpool UK, the United Kingdom Atomic Energy Authority (UKAEA), and the MIT Plasma Science and Fusion Center for deployment on MAST-U, with the goal of researching turbulent transport, and on DIONISOS for researching turbulence on the scale of the RF power source. Further applications of interest could be the measurement of astrophysical plasmas by satellites⁸ or in monitoring small laboratory or industrial plasmas.

ACKNOWLEDGMENTS

This work was supported by the Massachusetts Institute of Technology (supported by U.S. DoE Cooperative Agreement No. DESC0014264). The authors would also like to thank Chris Hickling for his effort in setting up and work on the collaboration for deployment of the MLP on MAST-U. The authors would also like to thank the reviewers for several suggested improvements to memory management to allow future experiments to save the real-time FPGA values at full precision.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

APPENDIX: FPGA MEMORY MANAGEMENT

The FPGA FIFO (First In First Out buffer) takes and transfers 32-bit data. The first bit is used to denote whether the data are a current–voltage pair or the real-time plasma parameters, and the next five bits are used for a time stamp, leaving 26 bits for data.

Within the FPGA logic, the current and voltage are both represented as 14-bit signed numbers; therefore, a divide-by-2 is required on both to fit into the FIFO. Within the FPGA logic, each of the plasma parameters is represented with a 20-bit signed number, where one bit equates to 0.0156 eV, 0.0156 V, and 0.0003 A for T_e , V_f , and I_{sat} , respectively. Thus, in order to fit T_e , V_f , and I_{sat} into the 26 available bits, it is necessary to throw out bits.

It is known that the calculated temperature will be positive and below 60 eV due to the limitations placed on the calculation algorithm; thus, the first 8 bits (the sign bit and the 7 most significant bits) can be safely discarded converting it to a 12-bit unsigned number. Due to the 14-bit ADC used to digitize the signal, it is safe to assume that V_f and I_{sat} will not have significant information in the first 6 bits and thus can be represented by a 14-bit signed number.

Finally, it is necessary to remove the last 5 bits (equivalent to a divide-by-32) of floating potential and ion saturation current and the last 4 bits (equivalent to a divide-by-16) of temperature prior to being sent to the FIFO. The resulting values are rounded down, causing the perceived downshift in values observed in Figs. 6 and 7.

A possible simple solution to this problem that does not involve a loss of precision in saved data would be to give each of the temperature, the potential, the ion saturation current, the collected current, and bias their own 32-bit number with the first 3 bits used as a flag to differentiate them. This was not carried out as it would significantly reduce the duration of data acquisition due to more quickly filling the RAM, and it would cause the current–voltage pair to be asynchronous in time. A more complicated solution would be to store all of the full precision data in a 46-bit number on the FPGA, then splice 16 of the 46-bit numbers together, and then divide them into 23 32-bit numbers for transition to the RAM. The original 46-bit numbers could then be reconstructed on the RAM by the ARM processor. In reality, this would be accomplished via a “send and save” framework in order to limit the data actively stored on the FPGA.

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