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A FAST ANALOGUE TO DIGITAL DATA ACQUISITION SYSTEM

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A FAST ANALOGUE TO DIGITAL DATA ACQUISITION SYSTEM

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ABSTRACT

Plasma physics experiments are generally carried out in 'single shot' machines in which plasma is contained for periods from 50 μsec to 5 msec. Within this time, analogue measurements relating to the plasma density, temperature etc., have to be recorded and much of the resultant data then needs to be converted into a form suitable for analysis by computer. This paper presents a data acquisition system designed to fulfil all these requirements.

A four-channel system is described which accepts simultaneous signals on each input, These signals are subsequently converted to a digital form and recorded in a small ferrite core store. The maximum sampling rate is 200 kHz. The digitised waveforms thus recorded are in a suitable form both for data handling and processing by a computer.

Details of the analogue to digital and core store circuitry employed are given, and an example of a store output system using a standard interface is described.

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CONTENTS

1. INTRODUCTION

Many of the experiments in fusion research are carried out in plasma containment machines, in which plasma is contained for periods of a few microseconds up to several seconds; the majority of machines work in the range 50 μsec to 5 msec.

During the course of an experiment many such containment periods or 'shots' are produced, and each time the experimental data relating to that shot must be collected and recorded. The data recorded, varies from fixed data, such as 'shot' number, slowly varying data, e.g. charging rate of capacitor banks, to fast transient signals from say photomultipliers viewing the plasma during the containment period. Consequently many recording channels are required, each channel with suitable characteristics for the measurement with which it is associated.

Much of the resultant data then needs to be converted into a form suitable for quantitative analysis by computer. To meet these requirements a number of different techniques have been used[1].

Fixed and slowly varying data are recorded by conventional data logging equipment, the digital outputs being either transmitted on-line to a small computer or stored on paper or magnetic tapes.

The fast transient signals present more of a problem and are mainly displayed on oscilloscopes and photographed either on Polaroid Land film or 35 mm film. For subsequent computer analysis the films then have to be scanned manually or automatically[2] to convert them to a digital form.

Several important limitations arise in the use of these photographic methods. Experimental progress is impeded by the length of

time taken to extract meaningful results from the film records; and the techniques employed are usually costly in manhours. Furthermore in a multichannel system the equipment required is both cumbersome and expensive.

The system described in this paper was designed to replace the photographic techniques employed, with a more economic and direct method of recording fast transient data. A sampling technique is employed, in which the transient signals from the experiment are sampled at regular intervals throughout the containment period. Each sample is converted to a digital number and recorded before the next sample is required. Consequently, after the 'shot', the experimentalist has a digital recording of the waveform immediately available for computer analysis.

The system is made economically feasible by the development of an inexpensive analogue to digital converter, and the recent reduction in the price of commercial core stores.

2. BASIC SYSTEM

The basic data acquisition system can be considered as two integral parts interconnected by a ferrite core store for intermediate data storage. One subsystem interfaces the source of data - electrical signals from transducers on an experiment - to the core store input; and the other subsystem interfaces the core store output to whatever permanent data recording medium is chosen. This may be a local recording on paper or magnetic tape, or the data may be transmitted via data links to a central computer.

Since the nature of the core store input and output systems are quite different, two different methods of control are employed. Data

input to the core store is synchronized to the repetitive sampling rate chosen by the experimentalist, and is controlled by a sequence control unit, each sample being written into consecutive locations in the store.

Data output from the core store is controlled by a British Standard Interface[3]. This permits any data handling equipment fitted with this Standard Interface to be connected to the core store output.

When the output device is a computer, data can be read out at a time and rate dictated by the computer.

3. INPUT SYSTEM TO THE CORE STORE

3.1 General

Fig.1 shows a functional block diagram of the subsystem interfacing the experiment to the core store. It represents the major part of the overall system.

The number of channels provided was determined by the accuracy of measurement required and the 32 bit word length available on the core store. The accuracy of each channel had to be at least as good, preferably better than the 3% to 5% absolute measuring accuracy of the oscilloscope and photographic technique previously employed. To achieve this, a 7 bit analogue to digital conversion was considered suitable, giving an accuracy of approximately 1% of the full operating range.

Four analogue channels are provided, each channel consisting of an amplifier, a follow-and-hold circuit and an analogue to digital converter. The data from all four channels is connected in parallel to the input of the core store, which has a 32 bit word length and 256 addresses. Overall control of the data input is supervised by a

sequence control unit.

In the physical construction, the identical functions, for example the four follow-and-hold circuits, are contained within a single unit. Details of each unit are given in subsequent Sections

3.2 Sequence Control Unit

As mentioned in Section 2, the sequence control unit controls the sampling of the transient signals from the experiment, and the resultant data input to the core store.

The sampling is synchronised by trigger signals from the sequence control unit (Fig.1). All four channels take samples simultaneously, a sample being defined as an instantaneous reading of amplitude.

In the first system a relatively limited range of sampling was provided. A range of five independent settings for both the number of samples required and the interval between samples, viz:-

Number of samples	16, 32, 64, 128, 256
Sampling interval (μsec)	5, 10, 50, 100, 500

Thus, a signal with a duration of 1.28 msec can be sampled 256 times.

Fig.2 shows the waveforms generated in part of a sampling sequence. The sequence control unit generates a chain of trigger pulses (Fig.2a), the number and time interval corresponding to the ranges selected by the experimentalist. Pulse width is fixed at 4.5 μsec; this keeps the follow-and-hold in the hold mode (Fig.2c), allowing adequate time for the subsequent analogue to digital converter to complete a conversion. Both the follow-and-hold and the analogue to digital converter are triggered simultaneously. After 4.5 μsec the

number strobed into the output register of the analogue to digital converter (Fig. 2d) is ready to be transferred to the core store.

Fig. 2e shows the pulse train controlling the core store. In this case, the pulses from the sequence control unit are synchronised with those of Fig. 2a, but have a mark space ratio of 1:1. An address counter in the core store increments the address by one for each pulse input.

Consider the sequence from the first sample at t_1 (Fig. 2). The follow-and-hold circuits and analogue to digital converters are triggered at t_1. After 2.5 μsec (t_2), address number 1 is selected in the core store. At t_3 the digital number corresponding to the first sample in each channel appears at the analogue to digital converter output registers. These numbers are transferred to a buffer register, the analogue to digital converters being allowed to continue with the next samples, at t_4 (Fig. 2a). Finally, after a fixed delay of approximately 2.8 μsec, the staticised numbers from all four channels are written into location 1 of the core store (Fig. 2g).

A similar sequence then follows for all subsequent samples, the core store address being incremented for each sample. It should be noted that the output register of the analogue to digital converters masks the time taken to write data into the core store, i.e. the second sample is being taken before the first is actually written into the core store.

3.3 Quad Follow and Hold

This unit has four identical circuits which can be triggered simultaneously or independently. Each circuit has two modes of operation, the 'follow mode' in which the output follows the input, and the 'hold mode' in which the output is held at a voltage level

corresponding to the input at the time of a hold command.

The circuit used is basically a long-tail pair amplifier (Fig.3) with single-ended output from the second transistor TR2 driving a capacitor C1. The signal input is applied to the base of TR1, whilst the output across C1 is fed back to the base of TR2 via an F.E.T., TR3, and an emitter follower, TR4.

3.3.1 Operation

In the 'follow mode' any reduction in input voltage causes an increase in the collector current of TR2, discharging C1 until both TR1 and TR2 collector currents and base voltages are equal.

Similarly for an increase in input voltage, the collector current of TR2 decreases and the resistor R1 supplies charging current to C1 until TR2 collector current again equals the current in R1.

The output is taken at the junction of TR2 base and TR4 emitter, a low impedance point.

With the circuit switched to the 'hold mode', the capacitor C1 is disconnected from the long tail pair amplifier by diodes D1 and D2 (Fig.3). These diodes are switched to divert both resistor R1 current and collector current of TR2 from C1, leaving the capacitor charged with an instantaneous voltage level. This charge can only leak away via the high reverse resistance of D1 and D2 or the input current of the F.E.T., which results in a voltage with a very slow rate of change appearing at the output, until D1 and D2 are switched back to the 'follow mode'.

The accuracy of the holding voltage depends mainly on three factors:-

(i) The leakage currents of the diodes and the F.E.T., discharging or charging C1.

(ii) Simultaneous switching of D1 and D2. Any difference between the switching of D1 and D2 results in injection or subtraction of charge from C1.

(iii) The ratio of D1 and D2 capacitance to C1. By capacitor divider action a percentage of the switching waveforms is fed through to C1.

To avoid significant breakthrough when C1 has a low value e.g. 100 pF, D1 and D2 must be low capacitance diodes.

3.3.2 Performance

Feedback and the inherent balance of the long tail amplifier combine to make this a very accurate and versatile follow-and-hold circuit.

The feedback improves the linearity, increases the bandwidth and equally important, reduces the time taken for the output to 'catch-up' with the input after a hold period (the recovery time). The advantage of the long tail amplifier is that, since both TR1 and TR2 are carrying similar currents, a very small offset voltage is achieved between input and output. This offset can be reduced even further when the source impedance is made equal to the output impedance and transistors TR1 and TR2 are a matched pair.

Measurements carried out on a number of circuits with C1 equal to 1.0 nF (a suitable value for use in the system) have resulted in the following performance. For an undistorted output (measured with a sine wave) of ± 2.5 V the typical bandwidth was DC to 750 kHz. The maximum time taken to settle to a steady level when switching

from 'follow' to 'hold' mode was 150 nsec, and the maximum pedestal caused by switching resulted in a 45 mV step on a stored level of 2.5 V. (In relation to the system this is the follow and hold units' most significant error). Droop in the holding voltage was measured by the time taken for the output to droop 25 mV on signals in the operating range ± 2.5 V and the temperature range 0°-40°C. The minimum time recorded was 3.2 msec. This droop is insignificant since the system only requires hold times of 4.5 μsec. An important parameter when the system is operated at 200 kHz is the maximum recovery time, which must be less than 500 nsec - this was measured as 400 nsec for the full operating range ± 2.5 V.

Change in offset voltage between input and output with a source impedance of 1K was a maximum of 10 mV over the temperature range 0°-40°C.

3.4 Quad Analogue to Digital Converter

There are at present many different methods of converting analogue voltages into digital form[4]. Each of these methods has its individual advantages and disadvantages. For the analogue to digital converter used in this system the important design criteria were, low cost, fast conversion (approx. 5 μsec), and relatively low accuracy (1%-2%). Consideration of these criteria led to the ramp/counter method of conversion as the optimum method to employ in the system.

In the ramp conversion technique the input voltage is converted to a time interval during which a gate is opened allowing the passage of a representative number of pulses from a clock generator into a counter. The time interval is created by comparing the input voltage with a linear ramp, which is started coincident with the first pulse.

into the counter. When the ramp equals the input voltage, an output from the comparison device stops the counting process.

The ramp technique is one of the simplest methods, and requires very few precision components. By sharing the ramp and clock a relatively inexpensive multichannel converter can be constructed. Furthermore, conversion time and accuracy are directly related, the greater the number of binary bits required the longer the conversion time. Thus accuracy can be traded for conversion time. The limit on conversion time is set by the performance of the logic elements used, e.g. maximum clocking rate of the counter, response of the comparator etc.

3.4.1 Description

The basic converter consists of the following: a comparator, linear ramp generator, clock generator, counter, output register, and a number of control gates.

Four converters are contained within the unit (Fig.4). The simultaneous operation of the four converters permits the sharing of both the ramp and clock pulse generators, and results in an economy in the number of control gates required.

The clock pulse generator (Fig.4) is a single transistor crystal oscillator. A clock pulse frequency of 31 MHz is required in order that the maximum count of 128 (7 bits) can be reached within the 5 μsec available between samples.

The ramp generator fixes the operating range of the system and works between -2 V and +2 V, count 64 corresponding to 0 volts. Both the starting level (-2 V) and the slope can be varied in order to adjust the converter. Since the ramp is distributed, a low output

impedance is essential to minimise interaction between comparators.

High speed differential comparators are used, capable of response times of 40 nsec and voltage comparisons with a resolution of 5 mV.

3.4.2 Performance

The performance of a number of units was checked over the temperature range $0^{o}C$ - $40^{o}C$. Conversion time, measured from the trigger command to a settled reading in the output register, was a maximum of 4.5 μsec. This is adequate for a system sampling rate of 200 kHz.

Accuracy of the converter depends on two inherent sources of error. The conversion errors and the intrinsic uncertainty in the least significant bit of the output.

From measurements, the conversion errors amount to ± 15 mV or ± 0.4% of full scale. The digital error, to ± 1 least significant bit or ± 0.8% of full scale.

For a common input voltage, no significant differences were observed between the readings obtained from the four channels within each unit.

3.5 Core Store

Two identical core store assemblies are incorporated in the system storage unit. Each of these store assemblies contains a ferrite-core matrix and its associated read/write and selection circuitry. The two assemblies are combined to form a single unit, with a word length of 32 bits, and 256 storage locations. Read/write cycle time for the combined unit is 4 μsec minimum.

Two modes of address selection are provided. An 8 bit counter permits incremental addressing and is used in the system to input

data to the core store; as described in Sec. 3.2. Random access addressing is also permitted and the facility is used in conjunction with a British Standard Interface to output data from the core store.

Additional gating circuitry is included in the core store unit to provide a non-destructive read out.

4. OUTPUT SYSTEM FROM THE CORE STORE

4.1 General

As previously mentioned in Sec. 2, the standard interface incorporated in the core store permits a variety of output systems to be connected to the core store. The system chosen depends on the particular requirements of the experiment. With the system outlined in the following sections, it is proposed to transfer data on-line from a stellarator experiment to the main computer facility (KDF9) for processing.

Once the data is in the KDF9 (where it may be on a disc file or archived on magnetic tape) it can be accessed via COTAN[5], an on-line multiaccess system. COTAN provides the user with a set of commands which enable him to manipulate and edit files, execute interactive programs or initiate programs in a background stream.

The proposed output system connecting the core store to the KDF9 is as shown in Fig.5.

4.2 Proposed System of Data Transmission to KDF9.

The core store will be situated in the vicinity of the experiment together with a data logger, the latter being used for the fixed and slowly varying data required with each 'shot'. Part of the fixed data will actually relate to the 'shot' recorded in the core store,

for example: the switch settings of the sequence control unit, etc. A channel selector is used to switch either of these sources of data to a data transmission link.

In this system (Fig.5) the information from the data logger will be the first to be transmitted, the transfer being supervised by a British Standard Interface (B.S.I.). Following this, the channel selector will be switched and the whole contents of the core store read out in sequence from address 1 to address 256, each address being generated by the sequence control unit together with a B.S.I. command to read out the corresponding data. The data is fed out from the core store to a digit selector, which will switch around the 32 bits located at each address in blocks of eight; the output from the digit selector appears on eight wires as a sequence of four eight bit numbers. Each of these numbers corresponds to a data channel, i.e. channel 1, channel 2 etc. When the digit selector has finished its scan, a B.S.I. command will be sent back to the sequence control unit to permit a change to the next address. After 256 similar cycles, the channel selector will switch back to the data logger source.

A parallel data transmission link is to be used to convey both the data and B.S.I. control signals to a small computer (PDP-8) approximately 400 metres from the experiment. The transmission link uses twisted pair cable and incorporates self-checking circuitry.

The PDP-8 computer (Fig.5) is connected on-line to several experiments and operates on a time-shared basis. It will be used with this system to perform some intermediate data processing. Preliminary data reduction and analysis will be carried out on the data received from the data logger, so that meaningful results, e.g. field strength of

a particular coil, can be sent back to the experimentalist immediately after the shot. Communication with the experimentalist is via a teletype terminal situated at the experiment (Fig.5). Furthermore, with the 7 bit words received from the core store, a program in the PDP-8 will add a parity bit to form 8 bit words. Every three consecutive words can then be packed to form two 12 bit words - thus enabling subsequent handling by the COTAN multiplexor.

A similar transmission link to that previously described (but with 12 bit capacity) will connect the PDP-8 to the COTAN multiplexor (a small computer) situated approximately 400 metres away at the KDF9 (Fig.5). This transmission link provides access to the computing power of the KDF9 together with all its peripherals.

COTAN information regarding the data being transferred to the KDF9 will be continually sent back to the experimentalist via the teletype link between PDP-8 and experiment. For example, the user may be informed of the number of sectors of disc file occupied by the data after each shot, etc.

In the event of a KDF9 or COTAN failure, all subsequent data received by the PDP-8 will be diverted to a buffer store (e.g. drum store) - thus avoiding delay in the progress of the experiment. With the data established in the KDF9, a normal COTAN terminal, direct from the KDF9 to the experiment, will enable the experimentalist to use a high level program language, e.g. FORTRAN, for his quantitative analysis of the data.

4.3 Progress in Implementing the Output System

At the present time, work is being carried out on both the hardware and software required to implement the proposed output system

(Sec.4.2). Most of the hardware has been tested, and the software required to handle the data via COTAN has been written and checked. However, before the entire system can be tested, a program for the PDP-8 has to be written and the overall control system proved as satisfactory.

5. CONSTRUCTION

A modular form of construction is used for the input system to the core store described in Sec.3. Each module, for example Quad analogue to digital converter, accommodates four channels and is built into a single width 8¾" (22.3 cm) NIM[6] module. The modules are plugged into a standard 19" (48.4 cm) NIM bin, which can accommodate 12 single width modules. The core store unit and the power supplies are accommodated in two separate chassis, both with the following dimensions: 19" (48.4 cm) wide, with a height of 7" (17.8 cm) and depth of 14½" (36.9 cm). All digital circuitry incorporated in the input system to the core store uses TTL integrated circuits.

The output system from the core store (Sec.4) comprises of both Culham and commercially designed equipment. Units situated at the experiment, such as channel selectors, data transmitter/receivers etc., are constructed with a standard width of 19" (48.4 cm). All of these units can be installed with the associated input units, core store etc., in a standard 19" (48.4 cm) rack.

6. CONCLUSIONS

The data acquisition system described above provides a direct communications link between the transducer outputs of a plasma physics experiment and the digital computer required for numerical analysis of these measurements. The tedious and expensive manual stages associated

with the photographic methods previously employed are eliminated, together with the costly equipment for measuring co-ordinates and digitising film. Furthermore, the time taken to extract meaningful results from the data, is significantly reduced.

For simplicity, the prototype system described has a limited range of sampling, supervised by a sequence control unit. The sampling sequence could be made more complex - say logarithmic - by using a digital timer[7] to provide the control pulses. Furthermore, a useful addition to the core store output would be a video display situated at the experiment, displaying the digitised waveforms in the core store for qualitative assessment.

The sampling technique used achieves an overall accuracy of between 1 and 2%, and a time resolution of 256 samples at 5 μsec intervals. This accuracy compares favourably with the previous photographic methods, but the resolution is not as good. For the system resolution, an information theory formula developed by Shannon[4,8] may be used as a basis of comparison. This formula shows that the minimum sampling frequency must be at least twice the signal bandwidth. Consequently, the system has a maximum bandwidth of 100 kHz whereas bandwidths of several MHz are possible with the photographic methods.

To improve the resolution of future systems using this sampling technique, two fundamental 'building blocks' must be improved. A multichannel analogue to digital converter with a conversion time of 200 nsec or less, and a backup store capable of accepting the data at such rates must be developed. Such a development can be envisaged using a parallel form of analogue to digital conversion, and MOS dynamic shift registers for storage.

7. ACKNOWLEDGMENTS

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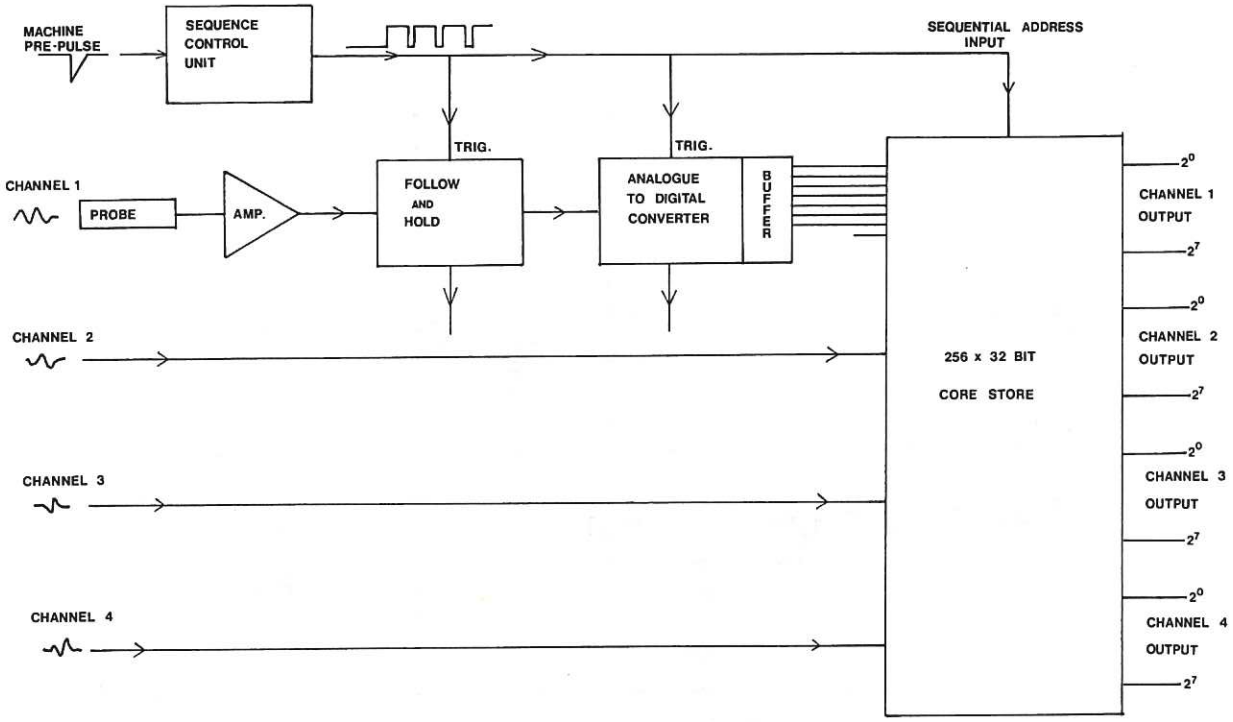

Fig. 1 Block diagram of input system to the core store

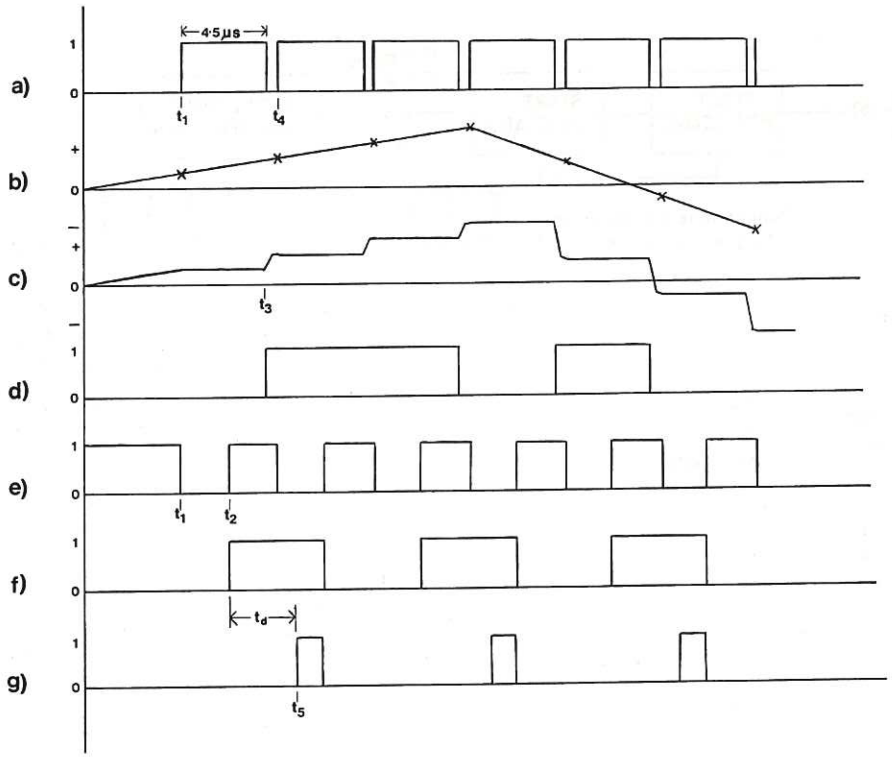

Fig. 2 Sequence control waveforms for 200 kHz sampling

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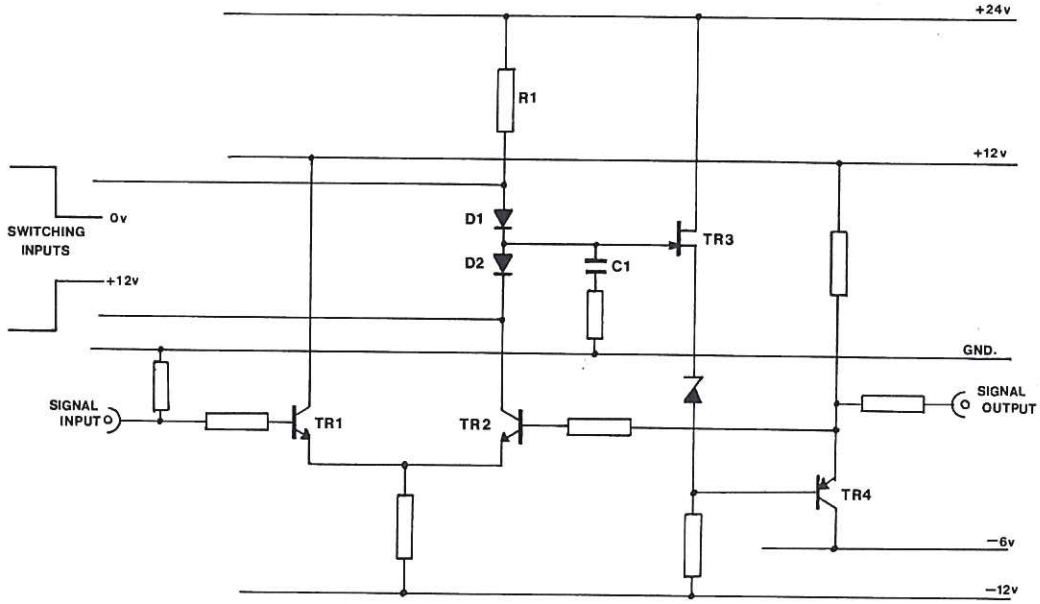

Fig. 3 Follow and hold circuitry

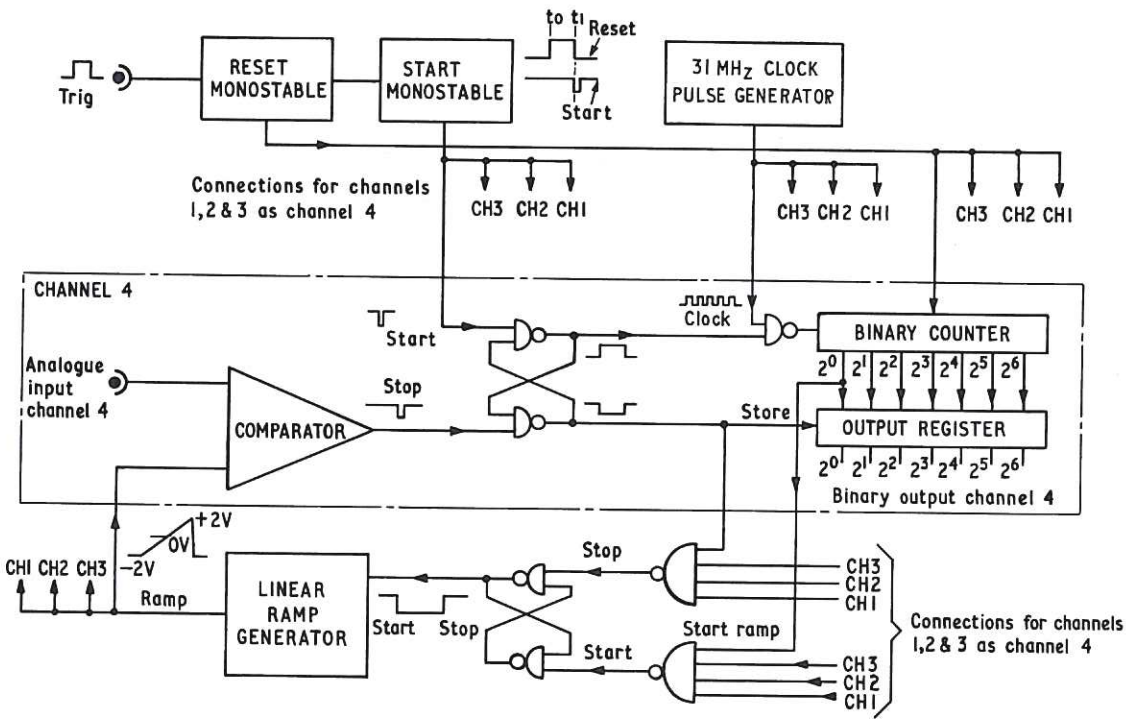

Fig. 4 Functional diagram of quad analogue to digital converter

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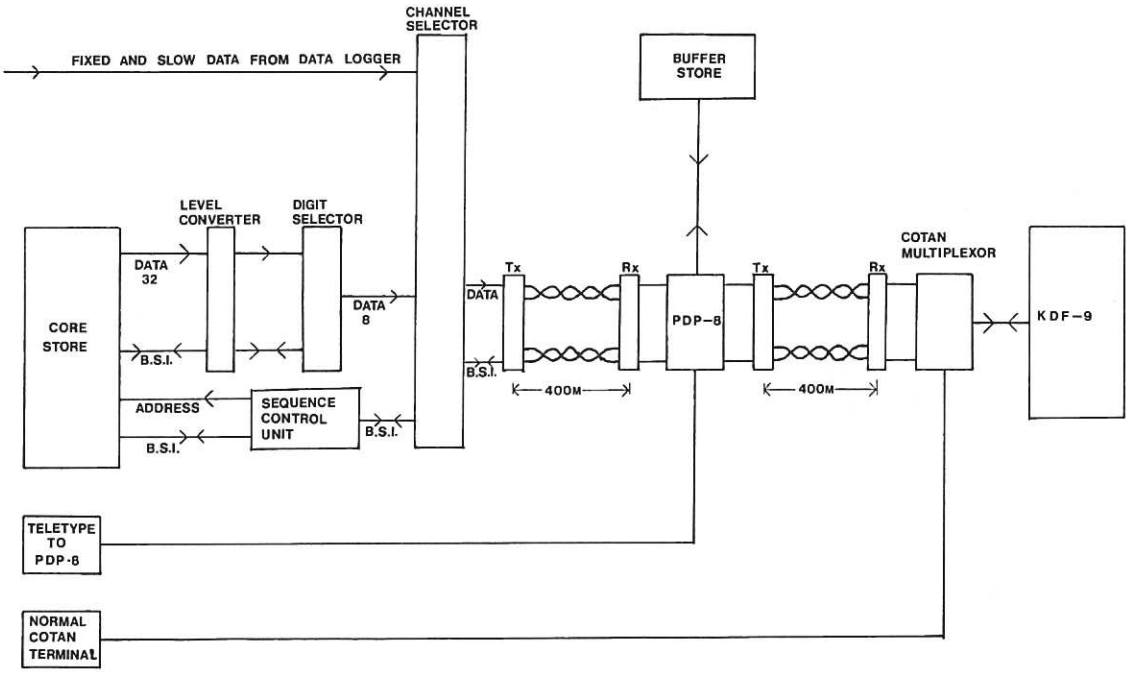

Fig. 5 Output system from core store CLM - P221