CLM-P 289

United Kingdom Atomic Energy Authority
RESEARCH GROUP
Preprint

AN ELECTRONIC CORRELATOR FOR FREQUENCIES OF 1 TO 100 kHz

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ABSTRACT

An electronic correlator for the frequency range 1 to 100 kHz is described. Time delays between 10^{-6} and 10^{-3} sec are produced by a lumped circuit delay line which is automatically switched. The output is plotted on a x y recorder.

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September 1971

1. INTRODUCTION

Correlation analysis is an extremely powerful technique with applications in many branches of science. In our particular field of interest, plasma physics, we are concerned with measuring the cross-correlation between two signals resulting from a pair of spatially separated detectors inserted into a plasma (Hooper, 1971). A wave propagating in the plasma thus appears in both signals as a coherent component with phase corresponding to the velocity of the wave and the separation of the two detectors. The coherent signal is usually swamped by a high level of incoherent noise resulting from the plasma itself as well as from the signal amplifiers, so that the coherence between the two signals is not generally apparent when they are displayed on an oscilloscope. By making an electronic measurement of the cross-correlation between the two signals we can deduce valuable information such as the velocity and direction of propagation of the wave in the plasma, the frequency and wavelength.

Suitable electronic correlators have recently become commercially available but are generally very expensive. There is a need for a cheaper but never-the-less accurate instrument and we describe such a device which we have built for the frequency range 1 to 100 kHz.

2. THE CORRELATION FUNCTION

The correlation function of two time varying signals x(t) and y(t) is defined mathematically as the time averaged value of the product of the two signals.

$$\langle x\,y(\tau)\rangle = \lim_{T\to\infty} \frac{1}{2T}\int_{-T}^{+T} x(t)\,y(t+\tau)\,dt\,.$$

A variable time delay τ is inserted into one of the signals so that the correlation may be plotted as a function of τ and thus any inherent time delay between the two signals can be resolved.

This is easily illustrated by considering a pair of sine waves of the same frequency ω which differ in phase by a fixed delay Δ, i.e.

$$x(t) = a_x \sin \omega t$$

$$y(t) = a_y \sin (\omega t + \Delta).$$

Thus: $$\langle xy(\tau)\rangle = a_x\, a_y \cos (\omega\tau + \Delta)\,.$$

The correlation thus appears as a cosine function of periodicity $2\pi/\omega$ and phase shift Δ which can be measured if $\langle x\,y(\tau)\rangle$ is plotted as τ is varied.

Waves of different frequencies or with random phase shifts will have zero correlations since the time integral over a long period averages to zero. Thus the correlation technique can be used to recover a weak coherent signal which is buried in random noise. The coherent part of the signal has a finite correlation whilst the noise averages out to zero.

It is also interesting to consider the special case of auto-correlations where a single signal is correlated with a time delayed copy of itself. Then:

$$\langle x\,x(\tau)\rangle = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{+T} x(t)x(t+\tau)\,dt \,.$$

The Wiener theorem relates the autocorrelation function to the power spectrum of the waveform by a Fourier cosine transform.

$$\langle x\,x(\tau)\rangle = \int_{-\infty}^{\infty} S_{xx}(\omega) \cos \omega\tau \, d\omega \,,$$

and

$$S_{xx}(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} \langle x\,x\,(\tau)\rangle \cos \omega\tau \, d\tau \,.$$

3. BASIC REQUIREMENTS FOR THE CORRELATOR

Three main stages are needed to compute electronically the cross-correlation function of two input signals.

(1) A variable time delay to delay one signal relative to the other.

(2) A multiplier to form the instantaneous product of the direct and the delayed signals.

(3) An integrator to carry out the time averaging of the multiplied signal.

The basic requirements for the time delay are determined by the operating frequency range, in this case 1 to 100 kHz. In order to accurately measure the correlation functions of near sinusoidal waves it is desirable to have a total delay of at least 5 cycles sub-divided into steps of at least one tenth of a cycle. Thus we would need a variable delay of 5 millisecs sub-divided into 1 microsec steps.

Physical size limits the practical use of delay cables to less than 1 microsec delays whilst magnetic tape systems are only economical for delays exceeding a millisec. Many commercial correlators use digital delay techniques coupled with a large number of hybrid analogue-digital multiplier elements. Such multichannel instruments are inevitably expensive. In order to build a simpler and cheaper instrument we use a single channel system with an artificial analogue delay line. The line is assembled from basic units with different characteristic delays and hence the working frequency limit falls as the longer delays are progressively switched in. The switching sequence is arranged so that only the higher frequency sections are used for short delays. The total delay available at any frequency is a minimum of 6 cycles between 6 kHz and 100 kHz. This is reduced below 6 kHz and falls to 1 cycle at 1 kHz, which is satisfactory for our purpose.

The delay line is automatically switched according to a pre-determined sequence in steps of 1, 2, 5, 10, 20 etc microsecs. After reaching a new delay value, the delayed and direct signals are multiplied and integrated for an integration period of a few seconds. The integrator output is then recorded on the y channel of an x y recorder whilst an analogue signal proportional to the value of the delay time is fed to the x channel. In this way a complete correlation is plotted automatically in one or two minutes depending on the length of integration time and the total number of points plotted.

4. DESCRIPTION OF THE CIRCUIT

A block diagram of the correlator is shown in Fig.1 and the main features are as follows.

4.1 Input Selection

Provision is made for up to five inputs out of which any pair say a and b may be selected for correlation by means of a pair of selector switches. A separate mode switch permits selection of the cross-correlations $\langle ab(\tau)\rangle$ or $\langle a(\tau)b\rangle$ or of the auto-correlations $\langle a\,a(\tau)\rangle$ or $\langle b\,b(\tau)\rangle$.

4.2 Pre-Amplifiers

Both the channels (i.e. the delay and the direct signals) are preceded by identical switched gain pre-amplifiers. Net gains of x100, x10, x1 and x0.1 are obtained from a x10 voltage gain amplifier together with either a second identical amplifier or 100:1 or 10:1 attenuators. The two x10 amplifiers are based on the buffer amplifier used in the delay line. The input impedance is 300 kΩ in parallel with 20 pF and the output impedance is 150 Ω. The attenuators have similar input impedance and are frequency compensated by capacitors.

4.3 Delay Line

This can be switched in steps of 1, 2, 5, 10 microsecs etc. up to 1 millisec by means of three miniature uni-selectors and is described in more detail later. The uniselector switches (A E I type 2200A) have the advantage of being relatively cheap and compact. They have better switching characteristics (i.e. very high off/on resistance) than semi-conductor switches and occupy much less space than would a comparable reed relay circuit. They have the usual disadvantages associated with mechanical switches, i.e. the contacts wear and need regular cleaning.

4.4 Buffer Amplifiers

A buffer amplifier is required in the delay channel so that a high impedance is presented to the delay line. An identical amplifier is included in the direct channel to preserve the symmetry. The same high z amplifier is used as within the delay line with the omission of R_3. (Fig.6(a)).

4.5 Drive Amplifiers

The multiplier input requires very low a.c. and d.c. source impedance, (less than 10 Ω). Operational amplifiers (Fenlow type AD 2000) are used as non-inverting amplifiers capacitively coupled to the preceding stage. Unity d.c. gain is used to minimize drift since a d.c. component in the multiplier input would produce a distorted output. The a.c. gain can be varied from x1 to x10 by means of a variable feedback resistor.

4.6 Multiplier

A commercial multiplier module (Fenlow MX 101) is used. This accepts input signals of either polarity up to ± 0.5 volt from d.c. up to 100 kHz. (Note however, that there is a.c. coupling at an earlier stage.) The multiplier operates in a four quadrant mode giving an output of correct sign:

$$y(t) = 2\,a(t)\,b(t)\ ,$$

where a(t) and b(t) are the input signals. Monitor sockets for the multiplier inputs are included to facilitate setting up the multiplier, and an output socket is available for connection to an external integrator.

4.7 Integrator

The integration:

$$Y = 4 \int_0^T y(t)\,dt\ ,$$

(T is in seconds) is effected using a µA 709 integrated circuit. An integrating time constant of 0.1 sec is given by a 1 µF capacitor and a 100 kΩ resistor. The integrator is preceded by a 10:4 attenuator, so that the maximum multiplier output of ± 0.5 volts integrated for 5 seconds will not exceed the output voltage range (± 12 volts) of the μA 709. Reed relays are used to reset the integrator and to gate the input.

4.8 Sample and Hold Circuit

A sample and hold circuit is used to eliminate sudden movement of the x y recorder pen back to zero each time the integrator is reset, the integrator output is sampled and stored on a 0.1 μF capacitor which is read out by a compound FET junction transistor emitter follower.

4.9 X-Axis Output

An output linearly proportional to the time delay is provided for the x-y recorder. A constant current source (1 mA) is fed to earth through a resistor chain which is switched by auxiliary contacts on the uniselector switches. A resistance of 10 Ω per microsecond of delay is used so that the x-output is 10 mV per microsecond. A large capacitor (20 μF) eliminates transients due to opening contacts.

4.10 Delay Line Switching Sequencer

Three uniselectors are used (Fig.2) each having three banks of twelve contacts. Contacts 0 - 9 of bank 'c' are used for switching the delay line, contact 0 - 9 of bank 'b' for switching the resistance chain and all the contacts, i.e. 0 - 11 of bank 'a' for controlling the operation of the uniselectors. A diode matrix is connected to bank 'a' and the position of the uniselector is indicated by an earth connected to the wiper marking the appropriate contact. The output of the matrix feeds into the switching circuit. The uniselectors are stepped by means of small thyristors. In the 1 μsec step position the 1 μsec uniselector's thyristor is triggered on the release of the 'step' relay (or the manual button) causing the uniselector to step on one contact. In the 2 μsec position the uniselector automatically steps over the odd numbered contacts and in the 5 μsec position over all except contacts 0 and 5. When contact 10 is reached the uniselector automatically steps on over contact 11 to contact 0 and in doing so steps the 10 μsec uniselector on one contact. Similarly the 10 μsec uniselector steps the 100 μsec uniselector on. When the 100 μsec uniselector reaches the tenth step the sequence stops, the resistance chain is set to zero, and the delay line output earthed thus setting x and y outputs to zero allowing the x,y recorder to plot the origin of the graph. When this occurs the visual display indicates ⦶⦶⦶ (the symbols 0 and 1 superimposed). In the x10 and x100 positions of the step selection switch the stepping pulse is fed to the 10 μsec and the 100 μsec uniselector respectively, and combined with the x2 and x5 switch the step size can be varied from 1 μsec to 500 μsec. Normally only the range 1 μsec to 20 or 50 μsec would be used. Each uniselector has a second thyristor. This is connected via the diode matrix to every contact of bank 'a' except contact 0. When they are triggered the uniselectors step automatically round to contact 0 thus resetting the delay line. Once the resetting action is initiated the time base is inhibited until all the uniselectors are at zero. Fig.3 gives the circuit for the 10 μsec uniselector. The 1 μsec and 100 μsec circuits are almost identical.

4.11 Display

This uses three 'Nixie' indicators. These are fed directly from the contacts of bank 'a' of each uniselector. The diodes of the switching circuit matrix serve to isolate the switching circuit from the + 250 V supply used for the 'Nixie' indicator.

4.12 Control and Limit Selection Switches

These are more or less self evident. The limits available are 5, 10, 100, 500 μsec and 'end'. The 'end' position allows the sequence to continue up to the Φ Φ Φ position. In the recycle position when the limit is reached and the last point has been plotted the delay line is reset and the sequence restarts. In the 'stop' position the integrator continues sampling but the delay line stays at a fixed position. In the 'run' position the delay line is stepped on each time. In the reset position the uniselectors are reset as described above.

4.13 Time Base

A block circuit diagram is shown in Fig.4(b). The integration timer consists of a uni-junction time delay circuit connected to a bistable. An incoming pulse from the reset integrator timer trips the bistable which starts the uni-junction circuit. When the uni-junction finally triggers, it feeds a pulse out to the sample and settling timers and resets the bistable. The time taken for the uni-junction to trigger can be varied from 0.2 - 5 secs by means of a potentiometer mounted on the front panel. The other four timers are simple monostable circuits. When the inhibit gate preceding the reset integrator timer is restored after the time base has been inhibited, it produces a pulse to restart the sequence. The settling timer delays the operation of the pen until the sample and hold circuit has had time to take up its new value.

The inhibiting gate for stopping and starting the time base is placed before the reset integrator timer to ensure that the integrator is fully discharged before any integration takes place. Also, when the time base is inhibited, the integrator is maintained in the reset condition once the cycle is completed.

A point is plotted for each value of delay selected from the one at which the sequence was started to the one at which it was stopped, thus if the sequence is stopped and restarted the point is repeated for the value of delay at which it was stopped.

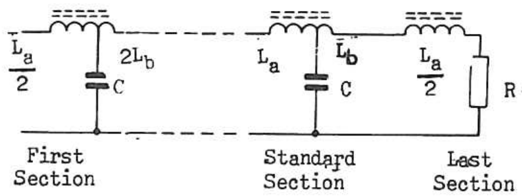
5. THE DELAY LINE

Basically this is intended to provide up to six cycles delay for any signal up to 100 kHz. Thus a maximum delay of 60 μsec is required at 100 kHz increasing to 6 msec at 1 kHz or 60 msec at 100 kHz. To keep the size of the line to reasonable proportions the maximum delay had to be limited to 1 msec (999 μsec). This means that 6 cycles of delay are only possible down to 6 kHz. Useful correlations can be made down to 1 kHz however.

The line is actually composed of twelve separate tapped delay lines each assembled on a plug-in printed circuit board. There are three groups, the first group (1 board) provides 9 steps of 1 μsec delay, the second group (4 boards gives 9 steps of 10μsec, and the third group (7 boards) gives 9 steps of 100 μsec. The output from each group is connected to a uniselector and the three uniselectors are then used to select the required delay. (Fig.2).

Each board contains a buffer amplifier driving a ten section artificial delay line. These sections are in effect low pass filters and the maximum frequency for which they can be used is inversely proportional to the delay per section. For frequencies close to the maximum, a minimum of about 20 sections are required to give 6 cycles delay. 40 sections would give 6 cycles delay down to half the maximum frequency and so on. Thus if all the sections were identical at least 400 would be required to give the required results. On the other hand there is no point in providing anything greatly in excess of 6 cycles delay for any particular frequency, i.e. for the longer delays the maximum frequency passed by the section can be reduced giving a longer delay per section. Using such a 'graded' line only 115 sections were necessary. Fig.5 shows the relation of delay to maximum frequency obtained. The 0 - 9 μsec delay, being designed for increments of 1 μsec rather than for a given maximum frequency, has a response exceeding 100 k Hz.

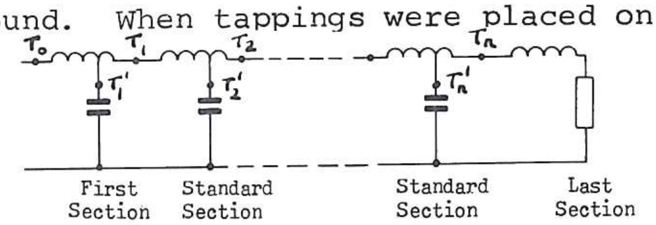
The line is based on the Pierce circuit as described by Wallis (1952)



$$La = rLb\ ,\ Lb = \frac{R\,T}{(\sqrt{r}+1)^2}\ ,\ c = \frac{T}{R}\ ,\ f_c = \frac{1}{\pi T}\frac{(\sqrt{r}+1)}{(\sqrt{r}-1)}\ ,$$

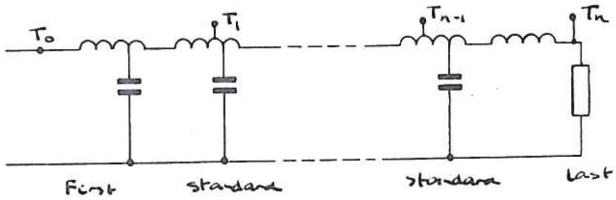
where T = low frequency time delay per standard section, f_c = the cut off frequency. With $r = 65$ the time delay is almost constant up to about 0.6 f_c. An alternative derivation is given in Appendix B which also demonstrates that the Pierce circuit is an M derived line, a point not made by Wallis.

The various lines were designed to this circuit and the coils wound. When tappings were placed on a completed line:-

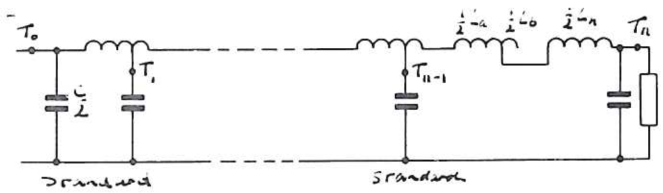


it was found that between T_1, and T_2, T_2 and T_3 etc, and between T_1' and T_2', T_2' and T_3' etc, there was a whole unit of delay, whilst between T_0 and T_1 or T_1' there was only about 0.6 of a unit.

On consideration it became apparent that the taps should be placed almost at the middle of L_a:-



However all the coils had been wound. Rearranging the circuit:-



gave a whole unit of delay for each step but gives greater mismatch with the termination R as f_c is approached. This causes the amplitude of the signal, at the taps, to vary with frequency. On test it was found that this did not exceed 3 dB up to 0.6 f_c. On future designs a tapped L_a should be used or the last section rearranged to give a better matching. (See Appendix C.)

TABLE I

CONSTRUCTION OF THE FIVE TYPES OF BOARD

Type	Quantity	Delay/ Section	Number of Sections	f_c	R
A	1	1 μsec	10	400 kHz	1 kΩ
B	4	25 μsec	10	160 kHz	1 kΩ
C	2	5 μsec	10	80 kHz	1 kΩ
D	3	10 μsec	10	40 kHz	1 kΩ
E	2	25 μsec	10	16 kHz	1 kΩ

Fig.6(a) shows the circuit of a board, Fig.6(b) the physical layout and Fig.2 the way the boards were interconnected to give the variable delay.

The buffer amplifier is basically a high input impedance (300 kΩ) low output impedance (50 Ω) gain of two amplifiers, the gain being determined by R 1 and R 2. R 3, shunted by Ra, increases the output impedance to 1 kΩ to match the line and the volt drop across R 3 reduces the overall gain to unity. Ra, of the order 20 - 100 kΩ, is selected on test to bring the output impedance to 1 kΩ ± 1%, before the link is connected. Rb, of similar value to Ra, is used to make the overall gain slightly greater than unity to compensate for the loss along the delay line (due to the resistance of the coils). The use of the high impedance buffer permits each succeeding line to be connected to the various taps of the previous line without effecting that line. Screened leads were used to make the connections between the taps and the uniselectors. The capacitance of these leads appears in parallel with the various capacitors c and $^{c}/2$. By a suitable layout it was possible to keep the error due to the lead capacitance to $< 1\%$, thus avoiding the need to make any correction for this in the values used for c (and $^{c}/2$).

6. CONCLUSION

Figures 7 and 8 show auto-correlation of sine waves from a signal generator. It can be seen that the correlator is still usuable although less accurate for delays longer than the designed six cycles.

We have measured the accuracy of the delay line by using an accurate digital frequency meter to determine at each delay step the frequency for which there is a 90° phase shift between the direct and delayed channels. This method thus takes account of any asymmetry between the two channels but only at the particular measurement frequency. Table II compares the measured delays with the nominal values. An accuracy of $\pm 1\%$ is obtained over most of the delay range, with errors increasing to $\pm 5\%$ for delays of

TABLE II

MEASUREMENT OF DELAY VALUES

Nominal delay µs	Measured delay µs	error %	Frequency for 90° phase shift kHz	Nominal delay µs	Measured delay µs	error %	Frequency for 90° phase shift kHz	Nominal delay µs	Measured delay µs	error %	Frequency for 90° phase shift kHz
1	1.048	+ 4.80	236.5	10	10.12	+ 1.20	24.71	100	99.76	- 0.24	2.506
2	2.15	+ 7.50	116.3	20	20.09	+ 0.45	12.44	200	199.20	- 0.40	1.255
3	3.19	+ 6.33	78.4	30	29.69	- 1.03	8.42	300	296.60	- 1.13	0.843
4	4.17	+ 4.25	60.0	40	39.81	- 0.47	6.28	400	388.20	- 2.95	0.644
5	5.15	+ 3.00	48.50	50	49.66	- 0.68	5.03	500	491.20	- 1.76	0.509
6	6.25	+ 4.16	40.0	60	59.34	- 1.10	4.21	600	589.60	- 1.73	0.424
7	7.35	+ 5.00	34.0	70	69.44	- 0.80	3.60	700	681.20	- 2.68	0.367
8	8.4	+ 5.00	29.7	80	79.22	- 0.97	3.16	800	781.25	- 2.34	0.320
9	9.4	+ 4.44	26.5	90	89.40	- 0.66	2.80	900	874.10	- 2.87	0.286

less than 10 μsec and greater than 800 μsec. We have found this acceptable for our purposes.

The instrument has been used successfully for correlation measurements on a plasma experiment. Fig.9 shows typical cross-correlations between a pair of probes separated around the azimuth of a cylindrical column of plasma. The frequency, wavelength, propagation velocity and azimuthal mode number of the plasma waves have been measured using the correlator.

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APPENDIX A

SPECIFICATION

Inputs Two channels designated a and b with identi- input parameters.

Range	0.1 mV to 1 volt (peak)
Impedance	300 kΩ shunted by 20 pF (150 kΩ 30 pF for auto correlation)
Coupling	a.c.
Frequency	1 to 100 kHz.

Function Cross-correlations $\langle a(\tau) b \rangle$ or $\langle a\, b(\tau) \rangle$

Delay time 1 to 1000 μsecs in 1 μsec steps.

Equivalent to 6 cycles delay at all frequencies above 6 kHz and reduced to 1 cycle delay at 1 kHz. This could be extended with an additional external delay unit.

Automatic switching of delay line in steps of 1, 2, 5, 10, 20 μsec etc. with single cycle or re-cycle facility.

Outputs

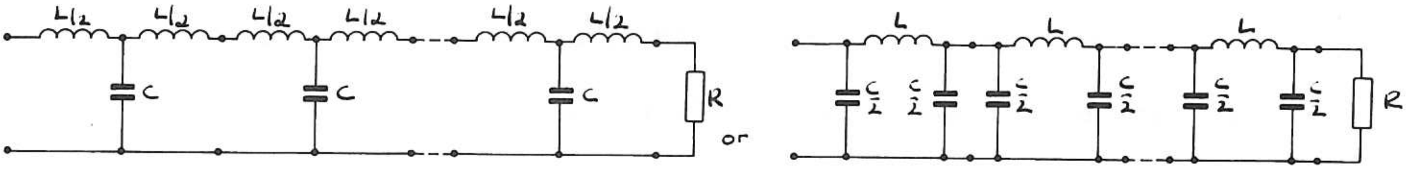
(i)	Multiplier output $y(t) = a(t)\ b(t + \tau)$	Impedance Level	Low ≃ 5 Ω ± 0.5 volts
(ii)	Integrated output $Y = \int_0^T y(t)dt$	Impedance Level	Low ≃ 150 Ω ± 12 volt

(iii)	Sample hold output y_{hold}	Impedance	Low $\simeq$ 150 Ω
		Level	± 12 volts
(iv)	x-axis output	Impedance	Varies with delay never more than 10 kΩ
		Level	10 mV/μsec for $\langle ab(\tau)\rangle$ -10 mV/μsec for $\langle a(\tau)b\rangle$
(v)	Pen control	Relay contacts closing for 50 msecs.	

APPENDIX B

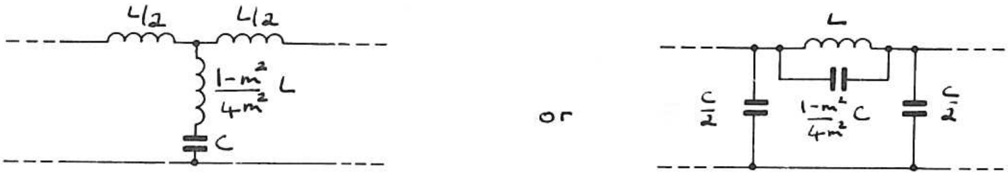
THEORY OF DELAY LINE

Artificial delay lines can be made from cascaded 'prototype' low pass filter sections of either T or π configuration where $L = R/\pi f_c$, $C = 1/\pi R f_c$, time delay



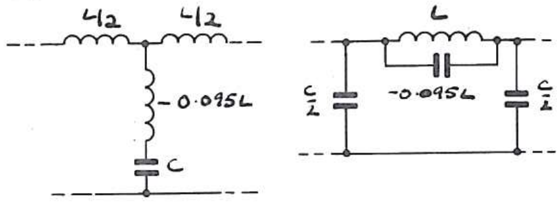
$(T) = \sqrt{LC}$ and f_c (the cut off frequency) $= 1/\pi\sqrt{LC}$. These types of lines only give satisfactory results up to about 0.2 f_c (Millman and Taub, 1956). Instead of the prototype sections 'm derived' ones may be used

L, C and f_c are the same as before but the delay per section t_m is now $m\sqrt{LC}$. Thus to retain the same delay as for a prototype section one would have to divide by m:-

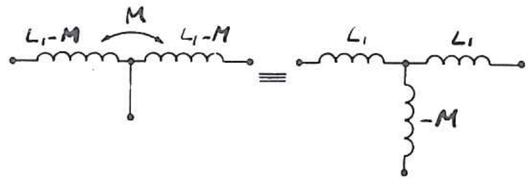


Now we have L, C and T as before but $f_c = m/\pi\sqrt{LC}$. If a value of $m \simeq 1.27$ is used a satisfactory performance up to 0.6 f_c is possible (Millman and Taub). For a given delay this is more than a three times improvement on the prototype section since f_c is 27% greater.

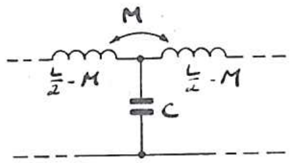
Substituting this value of m gives:



This requires either a negative value of L or C. Neither of these is directly obtainable but the effect of -L can be produced from the fact that



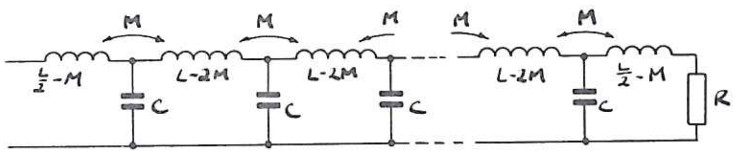
putting this in the 'T' type m section gives:



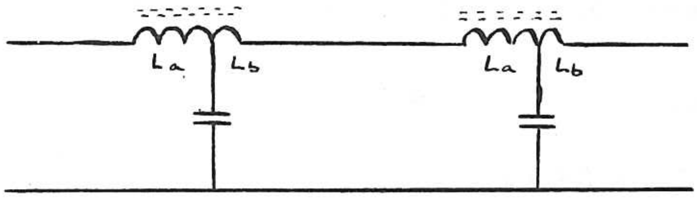
$$\text{with} \quad M = -\frac{1 - m^2}{4\,m^2} \cdot L$$

$$\text{i.e.} \quad M = \frac{m^2 - 1}{4\,m^2} \cdot L$$

When several sections are assembled into a line the two inductors that appear in series between each capacitor can be replaced by a single inductor of twice the value.



With air cored coils the mutual coupling can easily be arranged but, for the ferrite cored coils we require, it had to be provided by winding a few turns of one inductor on the core of the next. When there are two windings La and Lb on a core with 100% coupling their mutual inductance M is given by $M = \sqrt{La\ Lb}$. Consider a portion in the middle of the line.



Let $r = La/Lb$ then $La = rLb$ $\therefore$ $L - 2M = (r+1)\ Lb$

Also $M = \sqrt{LaLb} = Lb\sqrt{r}$ $\therefore$ $L - 2M = (r+1)M/\sqrt{r}$

but $M = (m^2 - 1)\ L/4m^2$

$\therefore$ $L - 2\ (m^2 - 1)\ L/4m^2 = \frac{(r+1)}{\sqrt{r}} \cdot \frac{(m^2-1)}{4m^2}$

$\therefore$ $4m^2 - 2m^2 + 2 = \frac{(r+1)}{\sqrt{r}} \cdot (m^2 - 1)$

$\therefore$ $2\sqrt{r}\ m^2 - r\ m^2 - m^2 = -\ 2\sqrt{r} - r - 1$

$\therefore$ $m^2(\sqrt{r}+1)^2 = (\sqrt{r}+1)^2$

$\therefore$ $m\sqrt{r} - m = \sqrt{r} + 1$ $\therefore$ $r = \left(\frac{m+1}{m-1}\right)^2$.

Writing $m = 1.27$ gives $r = 66$. We used a value of 64 which allows the use of an 8:1 turns ratio. This change has negligible effect since the change in m is less than 2% and frequency response only changes slowly with m around the value of 1.27.

$Lb(r+1) = L - 2M = L[1 - 2(m^2 - 1)/4m^2] = L[2 + 2m^2\ /4m^2]$

$\therefore$ $Lb(r+1)\ 4m^2 = 2L(1+m^2)$

but $m^2 = (\sqrt{r}+1)^2/(\sqrt{r}-1)^2$

$\therefore$ $Lb(r+1)\ 4(\sqrt{r}+1)^2/(\sqrt{r}-1)^2 = 2L[1 + (\sqrt{r}+1)^2/(\sqrt{r}-1)^2]$

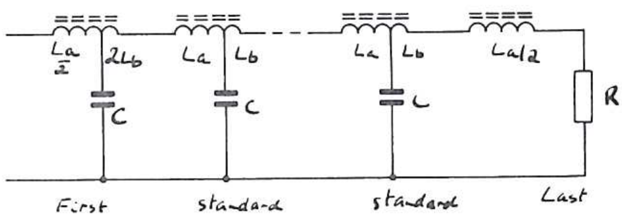
$\therefore \quad Lb(r+1)\,4\,(\sqrt{r}+1)^2 = 2L[(\sqrt{r}-1)^2 + (\sqrt{2}+1)^2]$

$\therefore \quad Lb = 2L[r+1 - 2\sqrt{r}+r+1+2\sqrt{r}]\,/\,4(r+1)(\sqrt{r}+1)^2 = 1/(\sqrt{r}+1)^2$

$\therefore \quad Lb = L/81 \quad \text{if} \quad r = 64$

$La = 64\,Lb = 64/81\,L$.

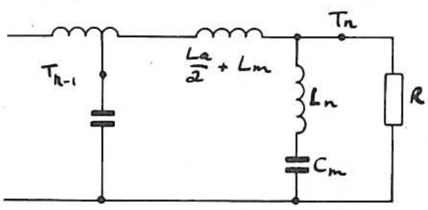
On drawing the complete line a problem occurs at the first and last coil. For the last inductor there is already the Lb of the previous coil present, so to give a total inductance of $La + Lb/2$, the coil requires an inductance of $La - Lb/2$. For the first inductor there is no Lb present so the main winding of the coil will have an inductance of $La + Lb/2$. To give the correct value of M the secondary will have to have an inductance that makes the product = La Lb, i.e. an inductance of $La\,Lb/[(La + Lb)/2]$ which $= 2\,Lb\,[La/(La + Lb)]$ which $\simeq 2\,Lb$ since $Lb \ll La$.
But the second coil in the line is designed for this inductance to be Lb not $\simeq 2\,Lb$. However, using the values below, the errors are less than 2%.



This is the Pierce line as described by Wallis (1952) ($la = L1$, $Lb = L2$, $R = Zco$ and $T = To$).

APPENDIX C

The effect of the re-arrangement approximates to placing 1.27 m half sections at the ends of the line. This gives poor matching to a resistive source or termination. Optimum matching occurs if a 0.6 m half section is used. To keep the delay correct a 0.6 m section can only be used at the end of the line and not at the beginning. This should be sufficient since if the end of the line matches the termination reflections will not occur. Such a termination is shown below.



$$L_m = \frac{0.6}{1.27} \cdot \frac{L}{2}$$

$$L_n = \frac{1-0.6^2}{4.0.6} \cdot \frac{1}{1.27} \cdot \frac{L}{2}$$

$$C_m = \frac{0.6}{1.27} \cdot \frac{C}{2}$$

This will cause some error in the delay at tap Tn. If this was more than 2% of the total an extra standard section would be necessary, so that the last tap would be before the matching network.

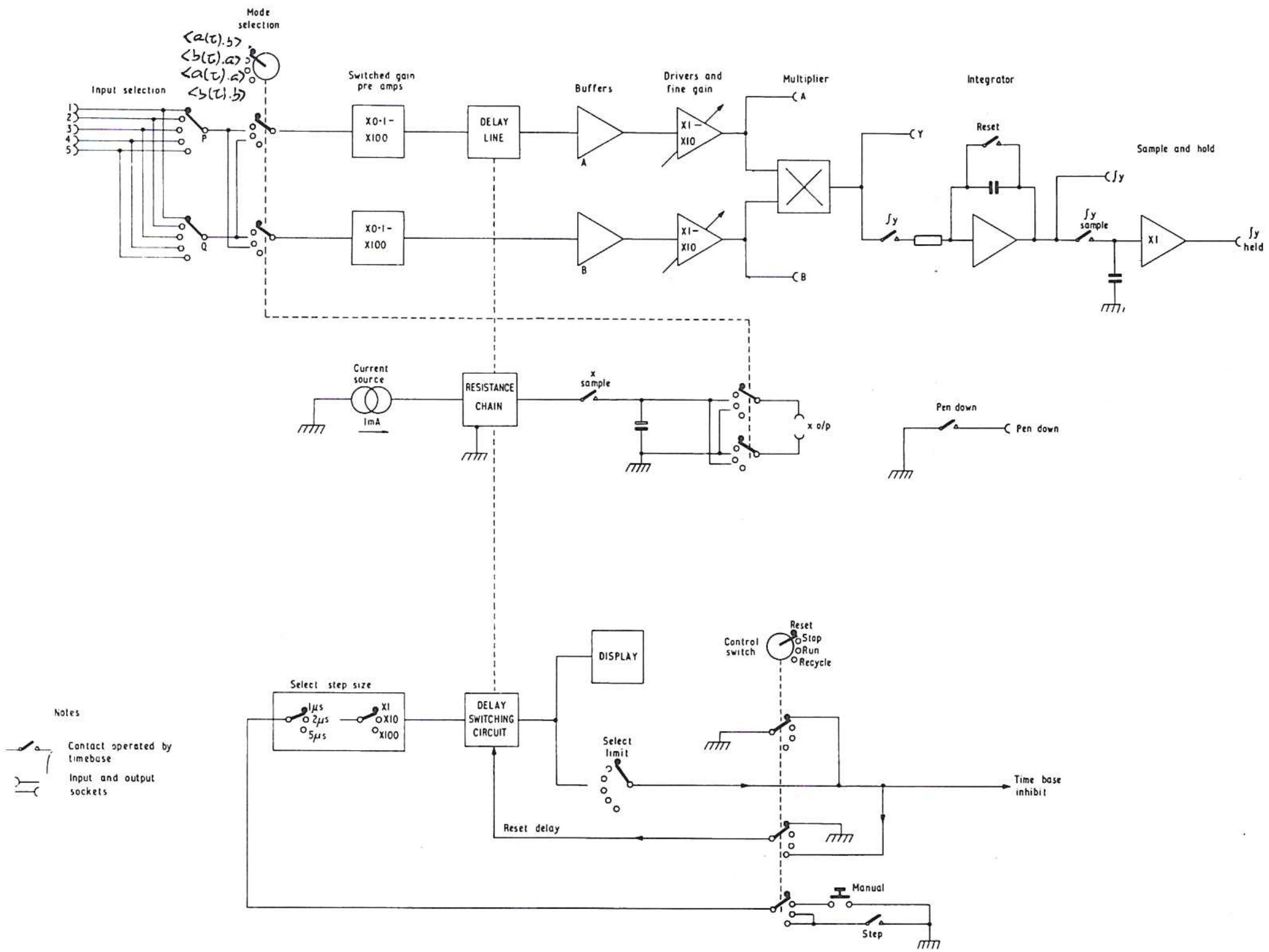


Fig.1 Block circuit diagram of the correlator.

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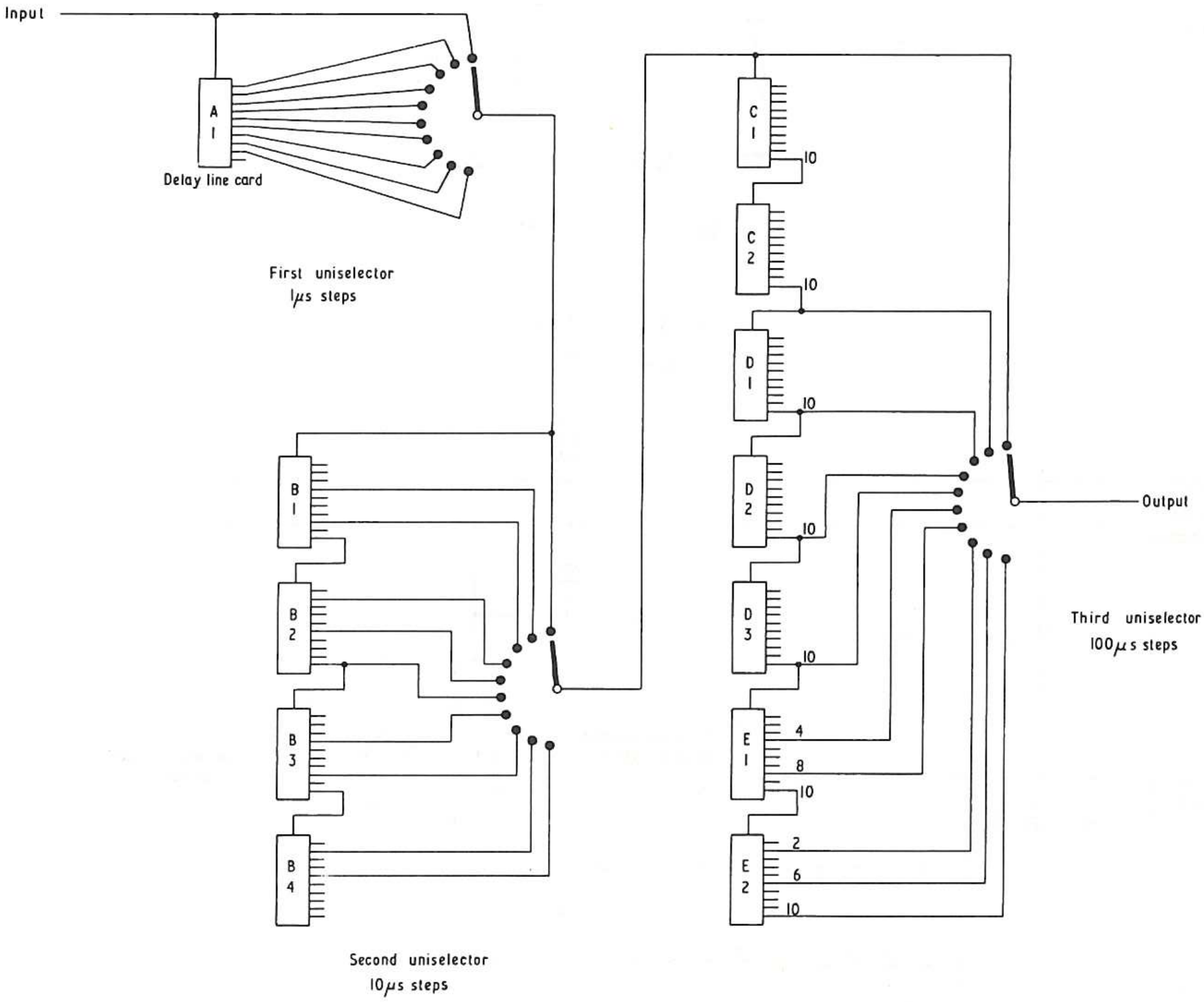

Fig.2 Block circuit diagram of the delay line.

CLM - P289

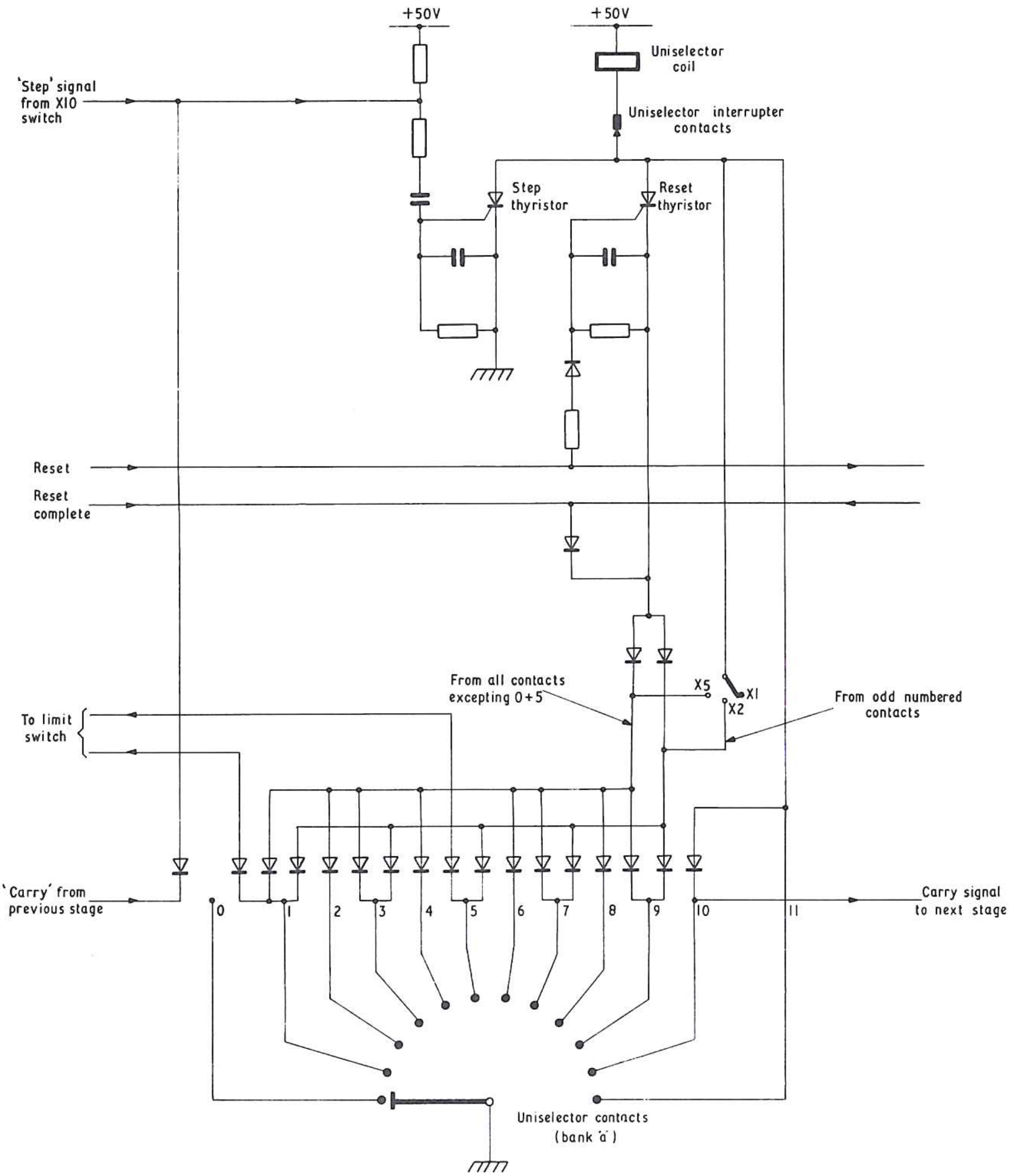

Fig.3 Current for the 10 μsec uniselector. The 1 μs and 100 μs circuits are almost identical.

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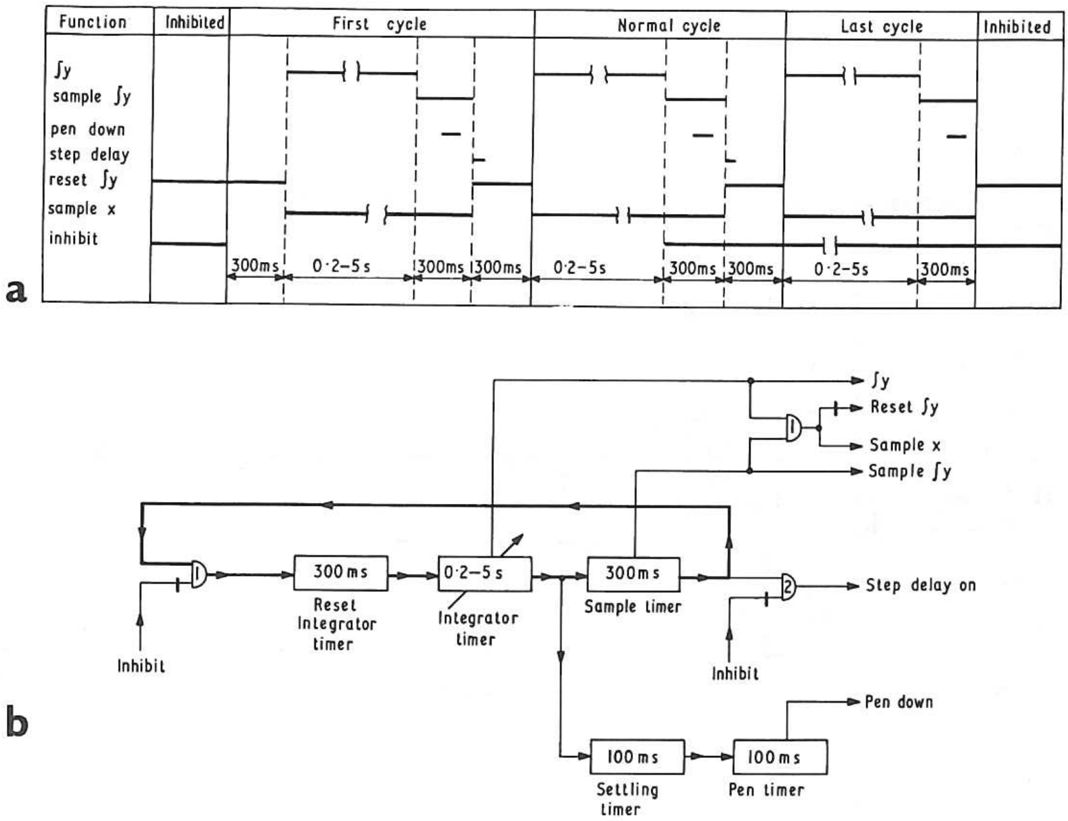


Fig.4 (a) Switching sequence of the delay line.
(b) Block circuit of the time base.

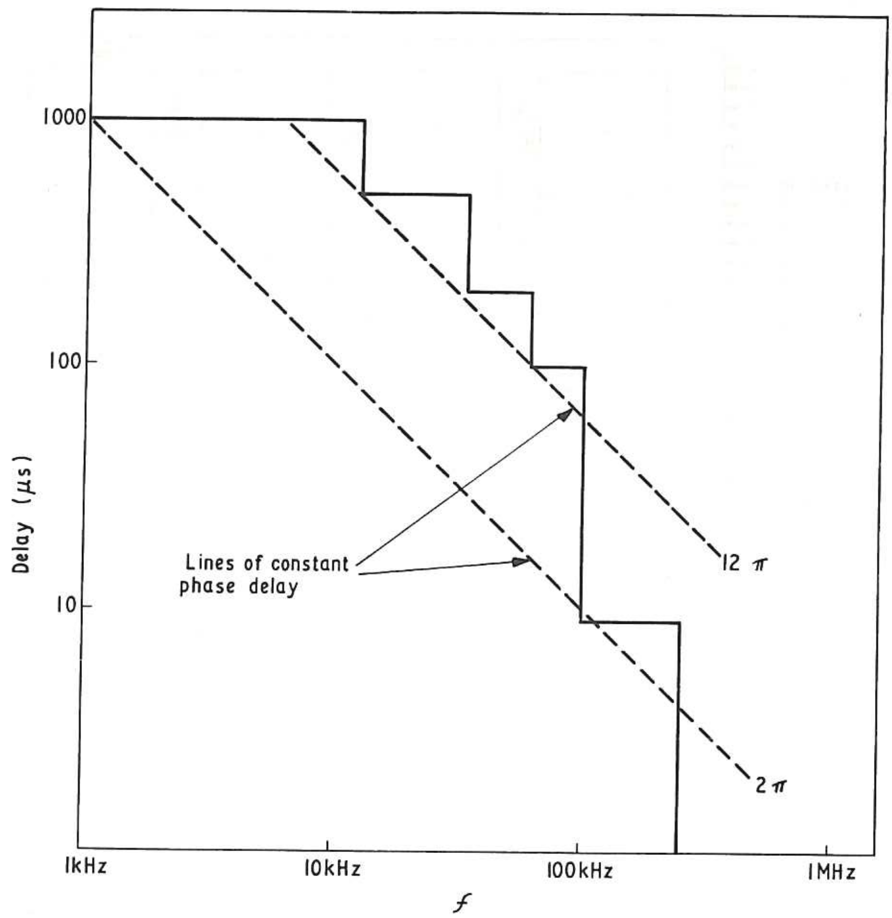
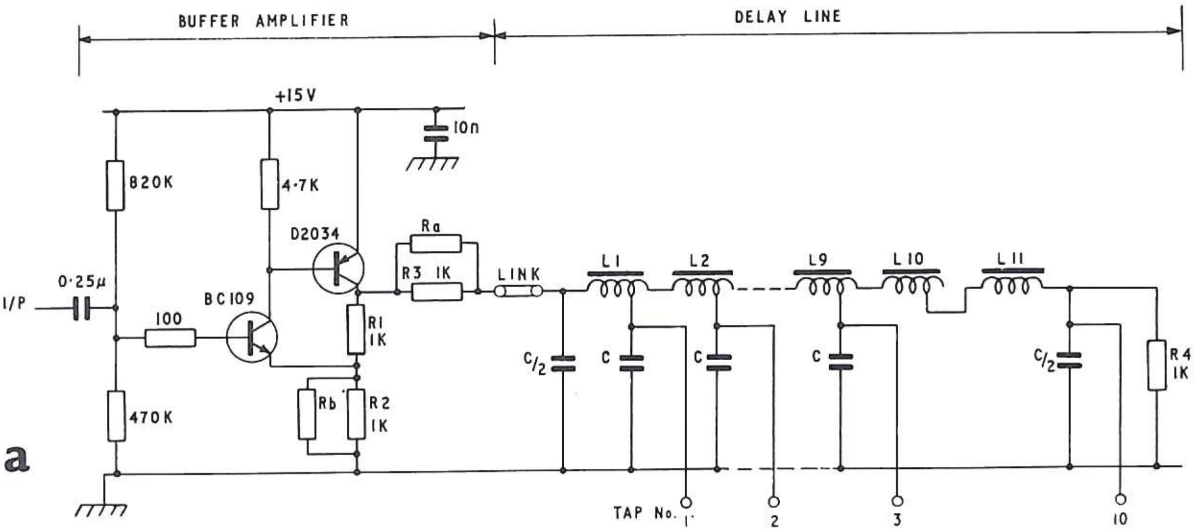


Fig.5 Relation of delay to maximum frequency obtainable.

a



b

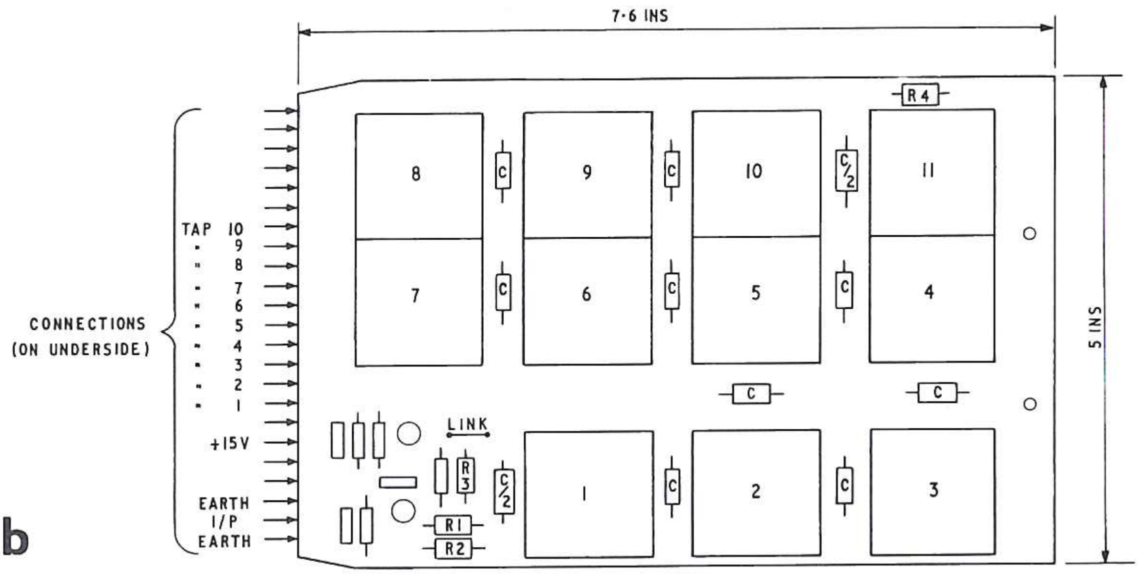


Fig.6 (a) Circuit of delay line plug-in board.
(b) Layout of delay line plug-in board.

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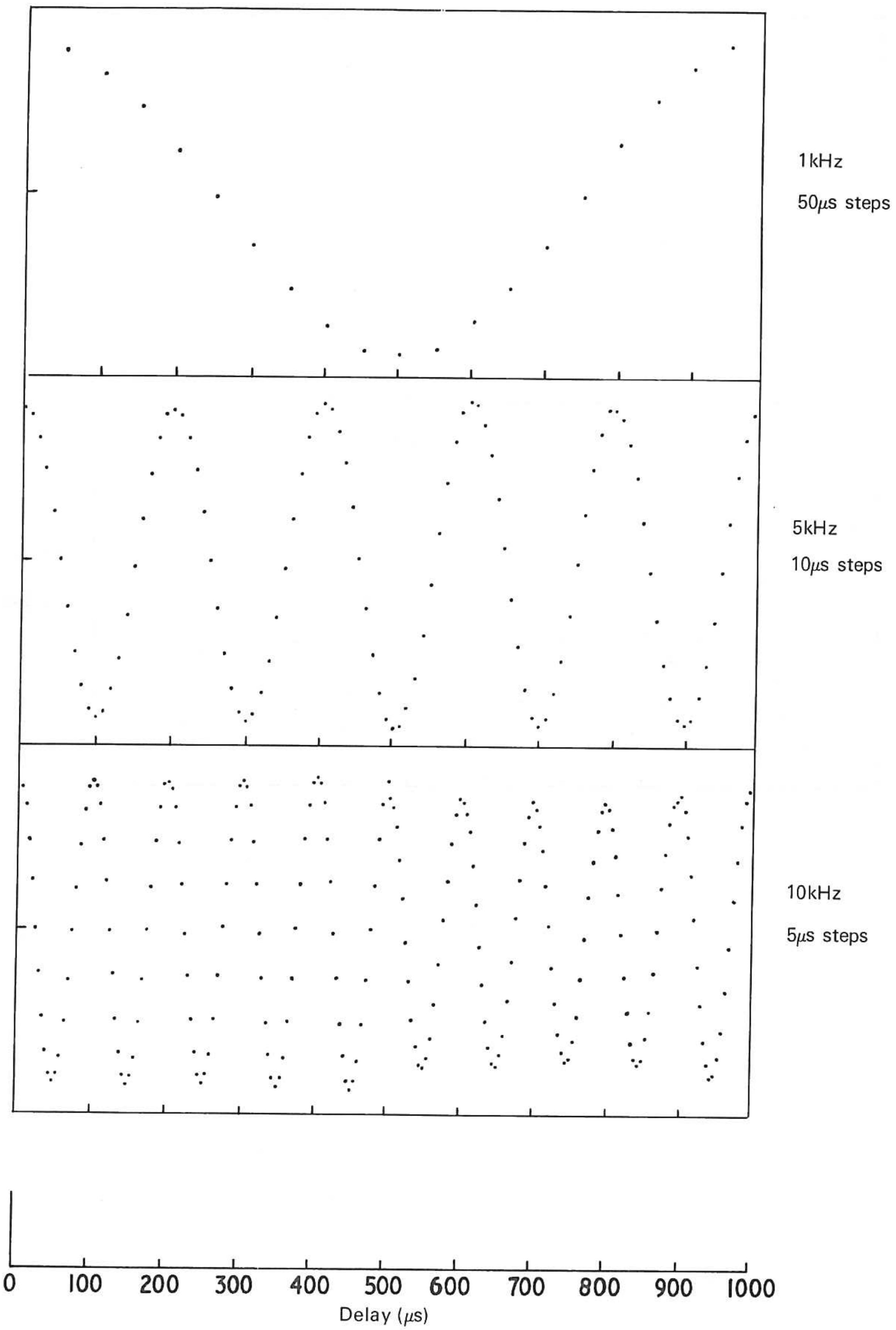

Fig.7 Autocorrelations of sine waves from a signal generator.

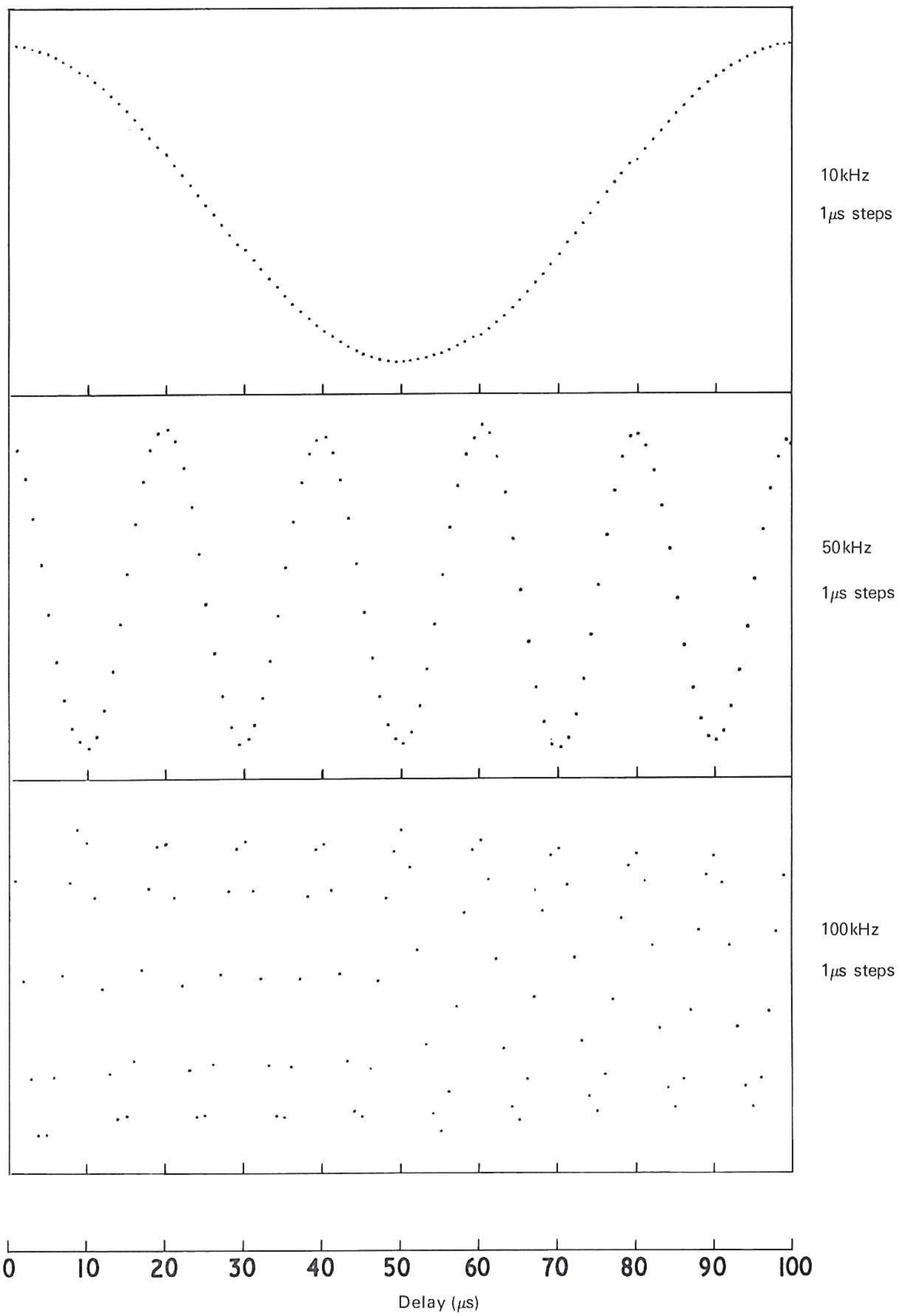

Fig.8 Autocorrelations of sine waves from a signal generator.

CLM - P289

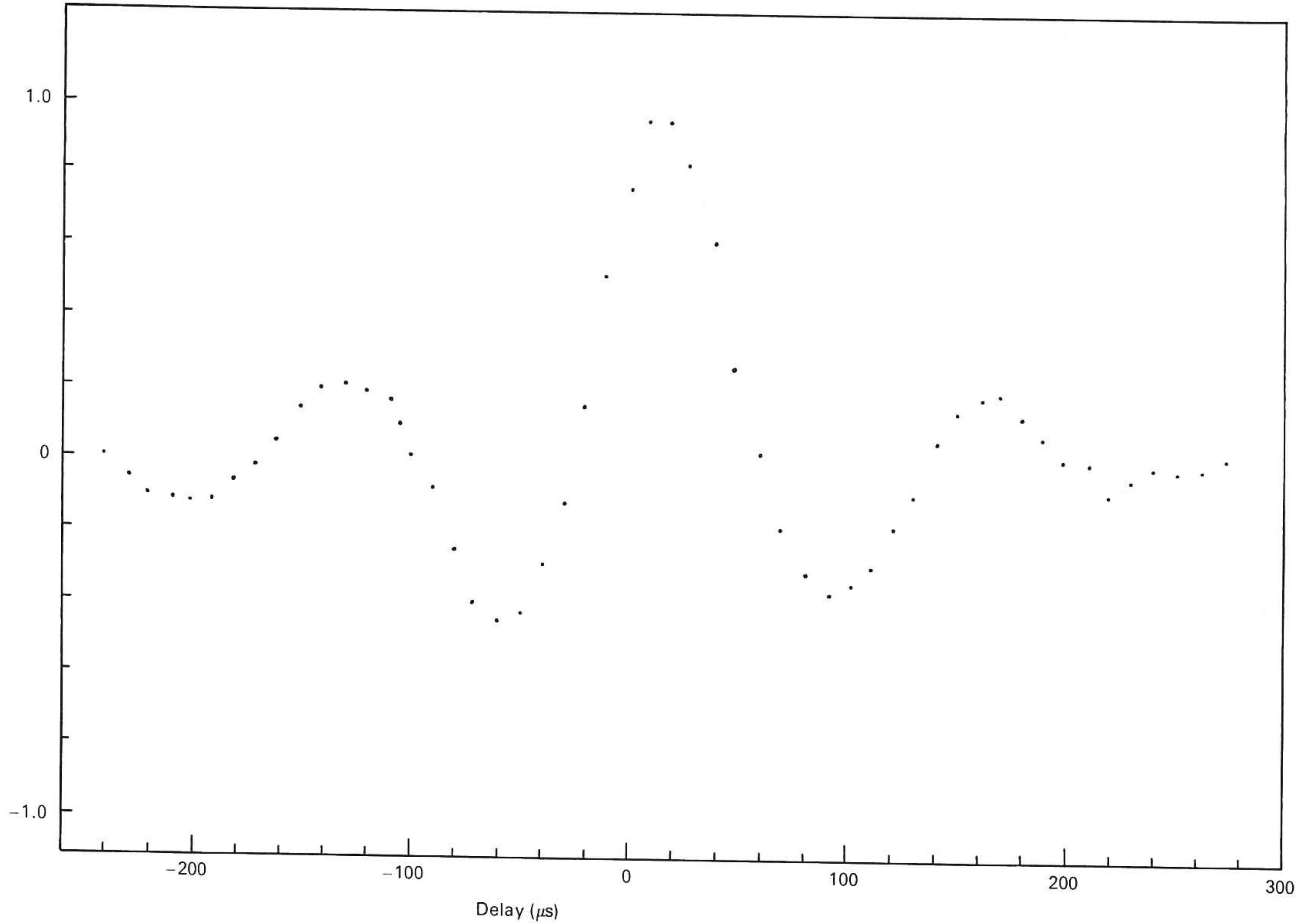

Fig.9 Typical cross-correlation between a pair of probes separated around the azimuth of a cylindrical plasma column.